IN THE UNITED STATES DISTRICT COURT

FOR THE DISTRICT OF DELAWARE

SAMSUNG ELECTRONICS CO., LTD., SAMSUNG ELECTRONICS AMERICA, INC., SAMSUNG TELECOMMUNICATIONS AMERICA GENERAL, L.L.C., SAMSUNG SEMICONDUCTOR, INC., and SAMSUNG AUSTIN SEMICONDUCTOR L.L.C.,	
Plaintiffs,	Civil Action No. 06-CV-0720 (***)
v.	
ON SEMICONDUCTOR CORP.	
and	
SEMICONDUCTOR COMPONENTS INDUSTRIES, LLC,	
Defendants.	

AMENDED COMPLAINT

Plaintiffs Samsung Electronics Co., Ltd. ("SEC"), Samsung Electronics America, Inc. ("SEA"), Samsung Telecommunications America General, L.L.C. ("STA"), Samsung Semiconductor, Inc. ("SSI"), and Samsung Austin Semiconductor L.L.C. ("SAS"), for their Amended Complaint against Defendants ON Semiconductor Corp. and Semiconductor Components Industries, LLC ("Defendants"), hereby demand a jury trial and allege as follows:

Parties

1. Plaintiff SEC is a corporation organized under the laws of the Republic of Korea, having its principal place of business at Samsung Main Building, 250, Taepyung-ro 2-ka, Chung-ku, Seoul 100-742 Korea.

2. Plaintiff SEC is in the business of manufacturing and selling a wide range of products. Specifically in relation to this action, SEC manufactures and sells dynamic random access memories ("DRAMs").

3. Plaintiff SEA is a New York corporation having its principal place of business at 105 Challenger Road, Ridgefield Park, New Jersey 07660.

4. Plaintiff STA is a Delaware limited liability company having its principal place of business at 1301 East Lookout Drive, Richardson, Texas 75082.

5. Plaintiff SSI is a California corporation having its principal place of business at 3655 North First Street, San Jose, California 95134.

6. Plaintiff SAS is a Delaware limited liability company having its principal place of business at 12100 Samsung Boulevard, Austin, Texas 78754.

7. On information and belief, Defendant ON Semiconductor Corp. is a Delaware corporation with its principal place of business at 5005 East McDowell Road, Phoenix, Arizona 85008.

8. On information and belief, Defendant Semiconductor Components Industries, LLC is a Delaware limited liability company with its principal place of business at 5005 East McDowell Road, Phoenix, Arizona 85008, is the principal domestic operating subsidiary of Defendant ON Semiconductor Corp., and does business under the name "ON Semiconductor."

9. Defendants manufacture and sell semiconductor products, including semiconductor components.

Nature of Action

10. In this action, Plaintiffs seek a declaratory judgment of noninfringement and invalidity of four United States Patents pursuant to the Declaratory Judgment Act, 28 U.S.C. §§ 2201 and 2202, and the Patent Laws of the United States, 35 U.S.C. § 100 *et seq.*, and such other relief as this Court deems just and proper.

11. This is also an action by Plaintiff SEC for patent infringement pursuant to the Patent Laws of the United States, 35 U.S.C. § 1 *et seq.*

Jurisdiction and Venue

12. This Court has subject matter jurisdiction over the subject matter of this action under 28 U.S.C. §§ 2201-02 and 28 U.S.C. §§ 1331 and 1338(a).

13. Venue is proper in this judicial district under 28 U.S.C. §§ 1391(b) and (c) and 1400(b) because Defendants reside in this judicial district.

The Patents

14. U.S. Patent No. 5,563,594 (the "'594 patent") entitled "Circuit and Method of Timing Data Transfers" was filed on August 31, 1994 and issued on October 8, 1996. Certificates of Correction issued on April 29, 1997 and March 22, 2005. The inventors named on the '594 patent are David K. Ford and Bernard E. Weir, III. A copy of the '594 patent is attached hereto as Exhibit A.

15. U.S. Patent No. 6,362,644 (the "'644 patent") entitled "Programmable Termination for Integrated Circuits" was filed on August 1, 2000 and issued on March 26, 2002. The inventors named on the '644 patent are Philip A. Jeffery and Stephen G. Shook. A copy of the '644 patent is attached hereto as Exhibit B.

16. U.S. Patent No. 5,361,001 (the "'001 patent") entitled "Circuit and Method of Previewing Analog Trimming" was filed on December 3, 1993 and issued on November 1, 1994. The inventor named on the '001 patent is David L. Stolfa. A copy of the '001 patent is attached hereto as Exhibit C.

17. U.S. Patent No. 5,000,827 (the "'827 patent") entitled "Method and Apparatus for Adjusting Plating Solution Flow Characteristics at Substrate Cathode Periphery to Minimize Edge Effect" was filed on January 2, 1990 and issued on March 19, 1991. The inventors named on the '827 patent are Virgil E. Schuster, Reginald K. Asher, Sr., and Bhagubhai D. Patel. A copy of the '827 patent is attached hereto as Exhibit D.

18. Defendants have represented that they own the '594, '644, '001, and '827 patents and have the right to sue for infringement.

19. U.S. Patent No. 5,252,177 (the "'177 patent") entitled "Method for Forming a Multilayer Wiring of a Semiconductor Device" was filed on July 29, 1991 with a foreign application priority date of April 15, 1991 and issued on October 12, 1993. A Certificate of Correction issued on September 19, 1995. The inventors named on the '177 patent are Jong-Seo Hong, Jin-Hong Kim, and Jung-In Hong. A copy of the '177 patent is attached hereto as Exhibit E.

20. Plaintiff SEC owns the '177 patent with the right to sue for infringement including past infringement.

Count I
(Declaratory Judgment Action for a Declaration of Noninfringement and Invalidity of U.S. Patent No. 5,563,594)

21. Paragraphs 1 through 20 are incorporated by reference as if stated fully herein.

22. Plaintiff SEC filed its original declaratory judgment Complaint in this action on November 30, 2006.

23. Defendants have accused SEC of infringing the '594 patent through its manufacture, sale, use, and/or importation of certain DRAMs, and have demanded that SEC license the '594 patent for exorbitant sums of money.

24. Defendants have informed SEC that they will not go away unless SEC enters into a patent license with Defendants, and SEC has informed Defendants that it will not pay Defendants the exorbitant sums they are seeking.

25. Because SEC had a reasonable apprehension that Defendants would file a patent infringement action against it for infringement of the '594 patent if SEC continued to manufacture, sell, use, and/or import certain of its DRAMs, and because an actual and justiciable controversy had therefore arisen between SEC and Defendants within the meaning of 28 U.S.C. § 2201, SEC filed its declaratory judgment Complaint in this action on November 30, 2006.

26. Thereafter, on December 4, 2006, Defendants made good on threats of litigation they made prior to SEC's filing of the original Complaint in this action, and filed their own action in the United States District Court for the Eastern District of Texas against Plaintiff SEC and its affiliated companies SEA, STA, SSI, and SAS for infringement of the '594 patent.

27. An actual and justiciable controversy within the meaning of 28 U.S.C. § 2201 exists between Plaintiffs and Defendants.

28. Plaintiffs have not directly or indirectly infringed any valid and enforceable claim of the '594 patent, either literally or under the doctrine of equivalents.

29. The '594 patent is invalid because of its failure to comply with one or more of the requirements of the patent laws of the United States, including, without limitation, 35 U.S.C. §§ 101, 102, 103, and/or 112.

30. A judicial declaration of noninfringement and invalidity is necessary and appropriate in order to resolve this controversy.

Count II
(Declaratory Judgment Action for a Declaration of Noninfringement and Invalidity of U.S. Patent No. 6,362,644)

31. Paragraphs 1 through 30 are incorporated by reference as if stated fully herein.

32. Plaintiff SEC filed its original declaratory judgment Complaint in this action on November 30, 2006.

33. Defendants have accused SEC of infringing the '644 patent through its manufacture, sale, use, and/or importation of certain DRAMs, and have demanded that SEC license the '644 patent for exorbitant sums of money.

34. Defendants have informed SEC that they will not go away unless SEC enters into a patent license with Defendants, and SEC has informed Defendants that it will not pay Defendants the exorbitant sums they are seeking.

35. Because SEC had a reasonable apprehension that Defendants would file a patent infringement action against it for infringement of the '644 patent if SEC continued to manufacture, sell, use, and/or import certain of its DRAMs, and because an actual and justiciable controversy had therefore arisen between SEC and Defendants within the meaning of 28 U.S.C. § 2201, SEC filed its declaratory judgment Complaint in this action on November 30, 2006.

36. Thereafter, on December 4, 2006, Defendants made good on threats of litigation they made prior to SEC's filing of the original Complaint in this action, and filed their own

action in the United States District Court for the Eastern District of Texas against Plaintiff SEC and its affiliated companies SEA, STA, SSI, and SAS for infringement of the '644 patent.

37. An actual and justiciable controversy within the meaning of 28 U.S.C. § 2201 exists between Plaintiffs and Defendants.

38. Plaintiffs have not directly or indirectly infringed any valid and enforceable claim of the '644 patent, either literally or under the doctrine of equivalents.

39. The '644 patent is invalid because of its failure to comply with one or more of the requirements of the patent laws of the United States, including, without limitation, 35 U.S.C. §§ 101, 102, 103, and/or 112.

40. A judicial declaration of noninfringement and invalidity is necessary and appropriate in order to resolve this controversy.

Count III
(Declaratory Judgment Action for a Declaration of Noninfringement and Invalidity of U.S. Patent No. 5,361,001)

41. Paragraphs 1 through 40 are incorporated by reference as if stated fully herein.

42. Plaintiff SEC filed its original declaratory judgment Complaint in this action on November 30, 2006.

43. Defendants have accused SEC of infringing the '001 patent through its manufacture, sale, use, and/or importation of certain DRAMs, and have demanded that SEC license the '001 patent for exorbitant sums of money.

44. Defendants have informed SEC that they will not go away unless SEC enters into a patent license with Defendants, and SEC has informed Defendants that it will not pay Defendants the exorbitant sums they are seeking.

45. Because SEC had a reasonable apprehension that Defendants would file a patent infringement action against it for infringement of the '001 patent if SEC continued to manufacture, sell, use, and/or import certain of its DRAMs, and because an actual and justiciable controversy had therefore arisen between SEC and Defendants within the meaning of 28 U.S.C. § 2201, SEC filed its declaratory judgment Complaint in this action on November 30, 2006.

46. Thereafter, on December 4, 2006, Defendants made good on threats of litigation they made prior to SEC's filing of the original Complaint in this action, and filed their own action in the United States District Court for the Eastern District of Texas against Plaintiff SEC and its affiliated companies SEA, STA, SSI, and SAS for infringement of the '001 patent.

47. An actual and justiciable controversy within the meaning of 28 U.S.C. § 2201 exists between Plaintiffs and Defendants.

48. Plaintiffs have not directly or indirectly infringed any valid and enforceable claim of the '001 patent, either literally or under the doctrine of equivalents.

49. The '001 patent is invalid because of its failure to comply with one or more of the requirements of the patent laws of the United States, including, without limitation, 35 U.S.C. §§ 101, 102, 103, and/or 112.

50. A judicial declaration of noninfringement and invalidity is necessary and appropriate in order to resolve this controversy.

Count IV
(Declaratory Judgment Action for a Declaration of Noninfringement and Invalidity of U.S. Patent No. 5,000,827)

51. Paragraphs 1 through 50 are incorporated by reference as if stated fully herein.

52. On December 4, 2006, after Plaintiff SEC filed its original declaratory judgment Complaint in this action on November 30, 2006, Defendants filed an action against Plaintiffs for

infringement of the '827 patent in the United States District Court for the Eastern District of Texas.

53. An actual and justiciable controversy exists between Plaintiffs and Defendants within the meaning of 28 U.S.C. § 2201.

54. Plaintiffs have not directly or indirectly infringed any valid and enforceable claim of the '827 patent, either literally or under the doctrine of equivalents.

55. The '827 patent is invalid because of its failure to comply with one or more of the requirements of the patent laws of the United States, including, without limitation, 35 U.S.C. §§ 101, 102, 103, and/or 112.

56. A judicial declaration of noninfringement and invalidity is necessary and appropriate in order to resolve this controversy.

Count V
(Patent Infringement of U.S. Patent No. 5,252,177)

57. Paragraphs 1 through 56 are incorporated by reference as if stated fully herein.

58. The '177 patent is valid and enforceable.

59. On information and belief, Defendants have infringed at least one claim of the '177 patent under one or more subsections of 35 U.S.C. § 271 through the manufacture, use, sale, offer for sale, and/or importation into the United States of certain of their products.

60. Plaintiff SEC has been damaged by Defendants' infringement of the '177 patent and will suffer irreparable injury unless the infringement is enjoined by this Court.

Prayer for Relief

WHEREFORE, Plaintiffs pray for judgment as follows:

A. That it be declared that Plaintiffs have not directly or indirectly infringed any claims of U.S. Patent Nos. 5,563,594, 6,362,644, 5,361,001, and 5,000,827 under any subsection of 35 U.S.C. § 271;

B. That it be declared that U.S. Patent Nos. 5,563,594, 6,362,644, 5,361,001, and 5,000,827 are invalid;

C. That Defendants have infringed U.S. Patent No. 5,252,177;

D. That Defendants, their officers, agents, and employees, and those persons in active concert or participation with any of them, and their successors and assigns be permanently enjoined from infringement, inducement of infringement, and contributory infringement of U.S. Patent No. 5,252,177, including but not limited to making, importing, using, offering for sale, or selling any devices or systems that infringe, or using processes that infringe, U.S. Patent No. 5,252,177 before the expiration of the patent;

E. That Plaintiff SEC be awarded all damages adequate to compensate it for Defendants' infringement of U.S. Patent No. 5,252,177, such damages to be determined by a jury and, if necessary to adequately compensate SEC for the infringement, an accounting, and that such damages be awarded to SEC with prejudgment interest;

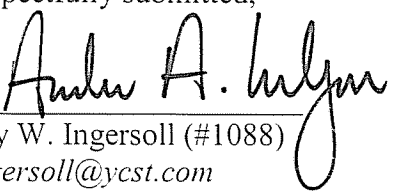
F. That this case be declared an exceptional case within the meaning of 35 U.S.C. § 285 and that Plaintiffs be awarded their attorneys' fees, costs, and expenses that they incur prosecuting this action; and

G. That Plaintiffs be awarded such other and further relief as the Court deems just and proper.

JURY DEMAND

Plaintiffs demand a trial by jury on all issues triable of right by a jury.

Respectfully submitted,



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Dated: December 21, 2006

CERTIFICATE OF SERVICE

I, Andrew A. Lundgren, Esquire, hereby certify that on December 21, 2006, the foregoing document was electronically filed with the Clerk of the Court using CM/ECF and served upon the defendants' registered agent as indicated below:

BY HAND DELIVERY

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EXHIBIT A

US005563594A

United States Patent [19]

Ford et al.

[11] Patent Number: 5,563,594

[45] Date of Patent: Oct. 8, 1996

[54] CIRCUIT AND METHOD OF TIMING DATA TRANSFERS

[75] Inventors: David K. Ford, Gilbert; Bernard E. Weir, III, Chandler, both of Ariz.

[73] Assignee: Motorola, Schaumburg, Ill.

[21] Appl. No.: 298,715

[22] Filed: Aug. 31, 1994

[51] Int. Cl.[6] H03M 9/00

[52] U.S. Cl. 341/100; 341/101; 327/279

[58] Field of Search 341/100, 101; 326/93; 327/160, 175, 265, 279

[56] References Cited

U.S. PATENT DOCUMENTS

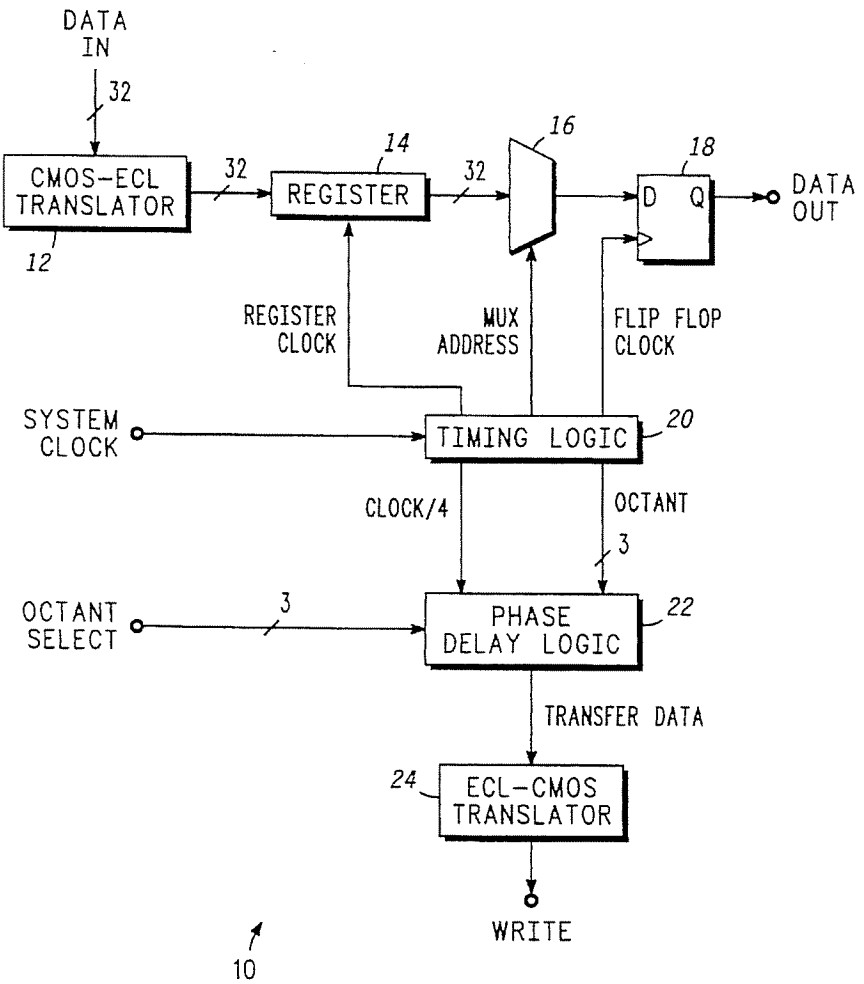
4,218,758	8/1980	Allen et al.	364/900
4,445,215	4/1984	Svendsen	370/279
4,815,107	3/1989	Kishimoto et al.	375/96
5,379,038	1/1995	Matsumoto	341/101

Primary Examiner—Marc S. Hoff
Attorney, Agent, or Firm—Robert D. Atkins

[57] ABSTRACT

A data conversion circuit receives input data from external sourcing logic and performs a parallel-serial conversion. Likewise, a data conversion circuit performs a serial-parallel conversion and presents output data to external sinking logic. In the parallel-serial conversion (**10**), the input data is translated (**12**) and stored in a register (**14**). A multiplexer (**16**) rotates through the data to provide the serial output. In the serial-parallel conversion (**70**), the input data is sequenced into a multiplexer (**74**) to achieve the parallel data word. The parallel data word is stored in a register (**76**) before presenting it to external logic. Phase delay logic (**22**) sets the delay of a transfer data control signal that requests data be read or written. Once the proper delay is determined by experimentation, the phase delay logic controls the phase of the transfer data control signal to request more data at the correct time, or present more data at the correct time, to allow maximum operating speed for the data converter.

19 Claims, 3 Drawing Sheets



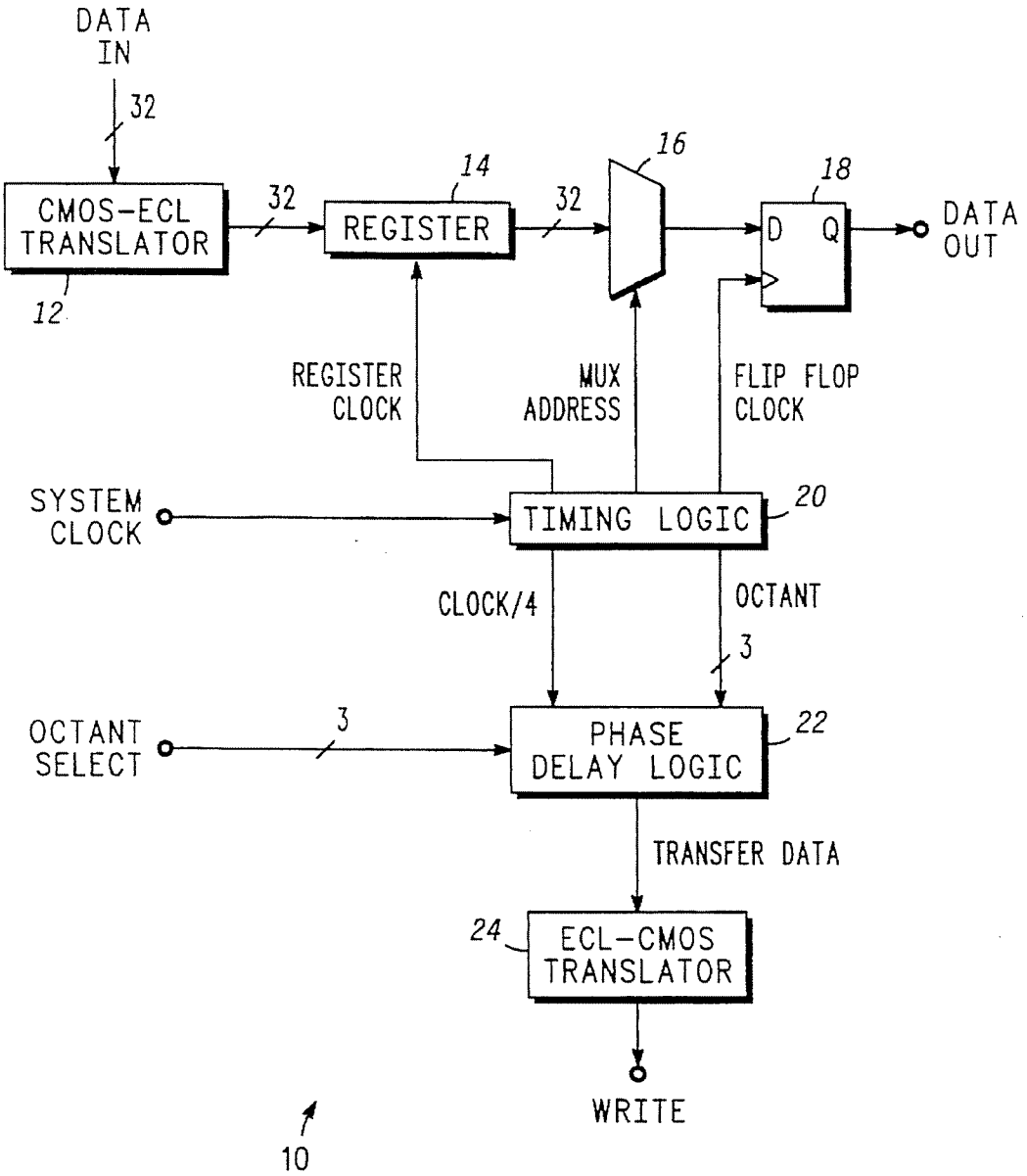

DATA IN
32
CMOS–ECL TRANSLATOR
12
32
REGISTER
14
32
16
18
D Q
DATA OUT
REGISTER CLOCK
MUX ADDRESS
FLIP FLOP CLOCK
SYSTEM CLOCK
TIMING LOGIC
20
CLOCK/4
OCTANT
3
OCTANT SELECT
3
PHASE DELAY LOGIC
22
TRANSFER DATA
24
ECL–CMOS TRANSLATOR
WRITE
10

FIG. 1

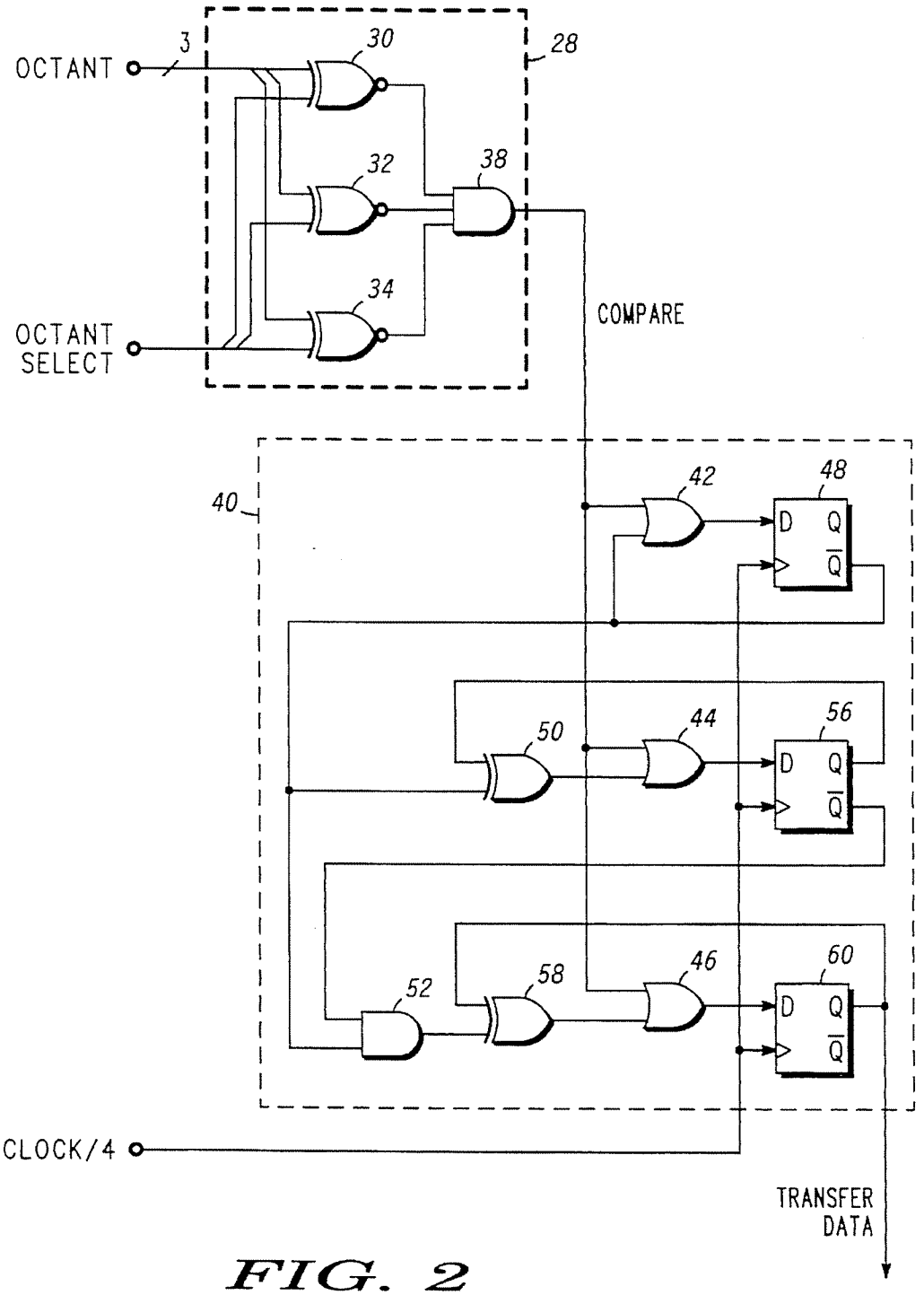

OCTANT
3
30
28
32
38
34
OCTANT SELECT
COMPARE
40
42
48
D
Q
Q
50
44
56
52
58
46
60
CLOCK/4
TRANSFER DATA

FIG. 2

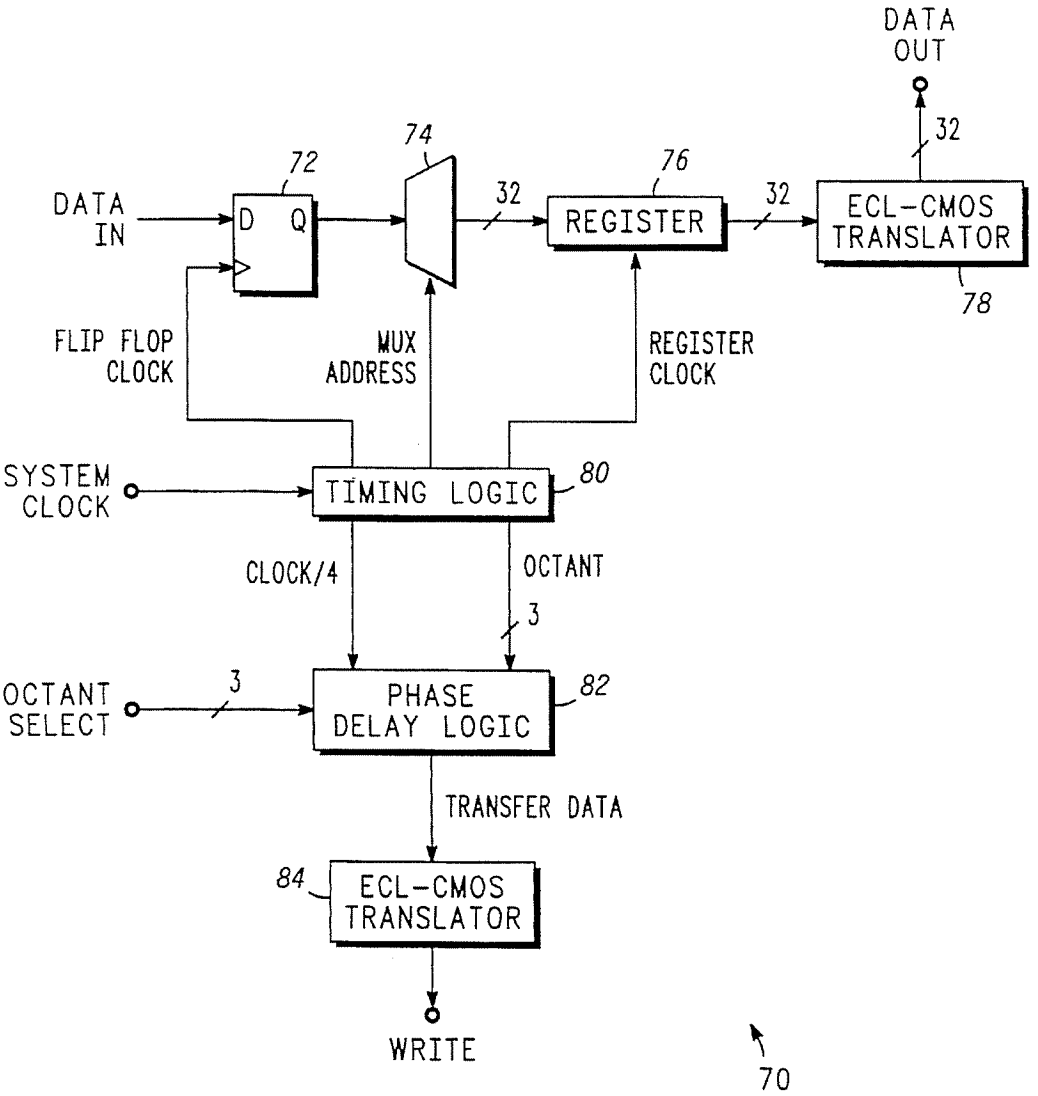

DATA OUT
32
74
72
76
DATA IN
D Q
32
REGISTER
32
ECL-CMOS TRANSLATOR
78
FLIP FLOP CLOCK
MUX ADDRESS
REGISTER CLOCK
SYSTEM CLOCK
TIMING LOGIC
80
CLOCK/4
OCTANT
3
OCTANT SELECT
3
PHASE DELAY LOGIC
82
TRANSFER DATA
84
ECL-CMOS TRANSLATOR
WRITE
70

FIG. 3

CIRCUIT AND METHOD OF TIMING DATA TRANSFERS

BACKGROUND OF THE INVENTION

The present invention relates in general to digital timing circuits and, more particularly, to controlling the phase of a data transfer signal to set the proper timing for reading or writing to a data register.

Parallel-serial converters are commonly used in digital circuit design to convert multi-bit signals to a string of data bits that are serially transmitted one at a time. Serial-parallel converters in turn convert the string of data bits back to multi-bit signals. In both applications, a data register is typically embedded within an integrated circuit that periodically receives new data sourced by external logic, or sources new data for external logic. Timing generation logic for reading or writing the data register is also embedded within the integrated circuit. The timing generation logic asserts a periodic signal to the external logic requesting data be presented to or removed from the data register.

Many applications involve high speed operation, say in the gigahertz range. The data transaction must be completed within a predetermined time period. That is, write data must be present and valid for a setup time before, and hold time after it is loaded into the register by a clock signal. Likewise, read data must be present and valid for a setup time before, and hold time after it is read by external logic. Unfortunately at such high data rates, the propagation delay uncertainties of the external logic are almost as long as the entire transaction period.

When the periodic signal is asserted to the external logic, requesting that new data be read or written, the external logic begins the time-consuming process of retrieving or storing new data. In the case of a request from the IC to the external logic to write new data, when the external logic finally presents new data to the integrated circuit, the new data typically propagates through buffer logic and eventually reaches the data register. The internal timing generation logic asserts a clock signal to load the data register. When the data transaction is so fast that propagation delay uncertainties consume almost the entire time period, there is no assurance that data arrives at the data register within register setup and hold-time constraints.

Since the write data register and timing logic are embedded within the integrated circuit, it is difficult to directly measure the actual write setup and hold-time. That is, the setup and hold-time are not readily observable by the external logic. If the write data setup and hold-time are unknown, the data rate of the external sourcing logic must be reduced to ensure sufficient setup and hold-time. Otherwise, where the propagation time uncertainty consumes a large portion of the transaction time period, the data transaction may fail to correctly time the data transfer under a worst-case timing analysis.

Hence, a need exists to properly set the timing of requesting more write data or read data for the data register to achieve maximum data transfer.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a block diagram illustrating a parallel-serial converter;

FIG. 2 is a schematic diagram illustrating the phase delay logic of FIG. 1; and

FIG. 3 is a block diagram illustrating a serial-parallel converter.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

Referring to FIG. 1, a parallel-serial converter **10** is shown suitable for manufacturing as an integrated circuit using conventional integrated circuit processes. A CMOS-ECL voltage translator circuit **12** receives a 32-bit DATA IN word from external sourcing logic (not shown) operating at CMOS logic levels. CMOS-ECL voltage translator circuit **12** provides a 32-bit signal operating at ECL logic levels to 32-bit register **14**. Register **14** loads data at rising edge of a REGISTER CLOCK signal. Multiplexer **16** rotates through the individual bit locations of register **14** under control of the MUX ADDRESS signal and provides serial bits to the data input of flipflop **18**. Flipflop **18** transfers the serial data signal to DATA OUT at its Q-output upon receiving a FLIPFLOP CLOCK signal.

Timing logic **20** operates in response to a SYSTEM CLOCK signal, running for example at 2.5 gigahertz, for providing the FLIPFLOP CLOCK signal and the REGISTER CLOCK signal. The FLIPFLOP CLOCK signal operates in phase and at the same frequency as the SYSTEM CLOCK. The REGISTER CLOCK signal is derived from dividing the SYSTEM CLOCK by value thirty-two. The REGISTER CLOCK signal is aligned on the same rising edge as the SYSTEM CLOCK. The MUX ADDRESS is reset to zero with each REGISTER CLOCK and counts up with the SYSTEM CLOCK to value thirty-two. Thus, the serialized data stream DATA OUT is sent at the SYSTEM CLOCK frequency with the duration of each serial bit time the same as the period of the SYSTEM CLOCK.

Timing logic **20** further provides a CLOCK/4 signal and a 3-bit OCTANT signal. The CLOCK/4 signal is derived by dividing the SYSTEM CLOCK by value four with alignment on the rising edges of SYSTEM CLOCK. The OCTANT signal takes one of eight binary encoded values (0 through 7) as seen in Table 1. During a first group of four consecutive SYSTEM CLOCKS C0–C3, OCTANT has a value "000". During the second group of four consecutive SYSTEM CLOCKS C4–C7, OCTANT has a value "001", and so on. The OCTANT signal changes state at each rising edge of CLOCK/4, for example, by incrementing a counter (not shown). Timing logic **20** includes combinational logic to divide the SYSTEM CLOCK and reset the MUX ADDRESS signal. Such combinational logic can be implemented from the aforedescribed operations.

TABLE 1

SYSTEM CLOCK	OCTANT
C0–C3	"000"
C4–C7	"001"
C8–C11	"010"
C12–C15	"011"
C16–C19	"100"
C20–C23	"101"
C24–C27	"110"
C28–C31	"111"

Phase delay logic circuit **22** receives CLOCK/4 and OCTANT signals from timing logic **20**, and an OCTANT SELECT signal from the external logic (not shown). ECL-CMOS translator **24** converts the TRANSFER DATA signal from phase delay logic circuit **22** to CMOS logic levels for the external logic. Upon receiving the WRITE control

signal, the external logic sends the next 32-bit DATA IN word.

It is important for the overall circuit operation that the output signal from REGISTER **14** does not become metastable. The 32-bit data at the output of translator circuit **12** must be stable for a finite "setup time" before the rising edge of REGISTER CLOCK. Likewise, the 32-bit data must remain stable for a finite "hold-time" after the rising edge of REGISTER CLOCK to ensure that register **14** clocks in valid data. Any violation of setup and hold-time may cause the register output to become metastable, yielding indeterminate logic levels for an indeterminate time duration.

Accordingly, as a feature of the present invention, phase delay logic circuit **22** sets the timing of TRANSFER DATA signal by altering its phase as programmed by the 3-bit OCTANT SELECT signal to request more data at the proper time to allow parallel-serial converter **10** to complete processing the previous data. In practice during a calibration sequence, the OCTANT SELECT signal may be set to various values to determine proper delay time necessary before the WRITE is asserted so that the next DATA IN word arrives at the optimum time to ensure proper data set-up and hold times at the input of register **14** and to allow time to complete processing the previous data. Once the proper delay is determined by experimentation, phase delay logic circuit **22** asserts the TRANSFER DATA signal at the correct time by controlling its phase to allow maximum operating speed for parallel-serial converter **10** given the required set-up and hold-time of register **14**.

Turning to FIG. **2**, further detail of phase delay logic circuit **22** is shown including a digital comparator **28** implemented as exclusive-NOR (XNOR) gates **30**, **32** and **34** and AND gate **38**. XNOR gate **30** receives bit**0** of the OCTANT signal and bit**0** of the OCTANT SELECT signal. XNOR gate **32** receives bit**1** of the OCTANT signal and bit**1** of the OCTANT SELECT signal. XNOR gate **34** receives bit**2** of the OCTANT signal and bit**2** of the OCTANT SELECT signal. The outputs of XNOR gates **32–36** are coupled to inputs of AND gate **38**. If the OCTANT signal matches the OCTANT SELECT signal, AND gate **38** receives all logic ones and provides a logic one COMPARE signal. Otherwise, the COMPARE signal from AND gate **38** is logic zero.

Logic block **40** provides a symmetric 50% duty cycle for the TRANSFER DATA signal by counting down after the COMPARE signal sets the TRANSFER DATA (most significant bit of three bit down-counter) to logic one. The COMPARE signal from AND gate **38** is applied to first inputs of OR gates **42**, **44** and **46**. The output of OR gate **42** is coupled to the D-input of flipflop **48**. The $\overline{Q}$-output of flipflop **48** is coupled to the second input of OR gate **42**, to an input of exclusive-OR (XOR) gate **50**, and to an input of AND gate **52**. The output of XOR gate **50** is coupled to a second input of OR gate **44** that in turn has an output coupled to the D-input of flipflop **56**. The Q-output of flipflop **56** is coupled to the second input of XOR gate **50**, while the $\overline{Q}$-output of flipflop **56** is coupled to the second input of AND gate **52**. The output of AND gate **52** is coupled to a first input of XOR gate **58** that in turn has an output coupled to the second input of OR gate **46**. The output of OR gate **46** is coupled to the D-input of flipflop **60**. The Q-output of flipflop **60** is coupled to the second input of XOR gate **58** and further provides the TRANSFER DATA signal to ECL-CMOS translator **24** in FIG. 1. Flipflops **48**, **56** and **60** receive the CLOCK/4 signal at their clock inputs.

During the 32-bit parallel to serial conversion, the 3-bit OCTANT signal increments on every rising edge of CLOCK/4, i.e. every four SYSTEM CLOCKS. When the 3-bit OCTANT signal matches the externally-supplied 3-bit OCTANT SELECT signal, the COMPARE signal is asserted as logic one. The Q-outputs of flipflops **48**, **56** and **60** go to logic one on the next rising edge of the CLOCK/4 signal. The TRANSFER DATA signal goes to logic one. When the OCTANT signal increments to its next value and COMPARE returns to logic zero, flipflops **48**, **56** and **60** operate as a 3-bit synchronous down counter and decrement with each rising edge of CLOCK/4. Since the TRANSFER DATA signal is the most significant bit of the down counter, it remains logic one for the first half of the counts and returns to logic zero for the second half of the counts. Logic block **40** thus provides a symmetric 50% duty cycle for the TRANSFER DATA signal.

For example, assume that the 32-bit DATA IN signal is latched into register **14** by the REGISTER CLOCK. In the present example, it has been determined by experimentation that the OCTANT SELECT signal "001" sets the proper phase delay before asserting TRANSFER DATA to the external logic to send the next DATA IN word. The delay determines the amount of time parallel-serial converter **10** needs to complete processing the present data word and be ready for the next. Assume that the Q-outputs of the flipflops begin at logic one and the $\overline{Q}$-outputs begin as logic zero. The first four SYSTEM CLOCKS C**0**–C**3** correspond to multiplexer **16** reading the four least significant bits D**0**–D**3** from register **14**. At the first rising edge of CLOCK/4 (clock C**0**), the OCTANT signal is "**000**" and does not match the OCTANT SELECT signal "001". Consequently, the COMPARE signal is logic zero.

At the second rising edge of CLOCK/4 (clock C**4**), the OCTANT signal switches to "001" and matches the OCTANT SELECT signal causing the COMPARE signal goes to logic one. The outputs of OR gates **42–46** go to logic one due to the logic one COMPARE signal for the initial state of the down count. Four SYSTEM CLOCKS later, the third rising edge of CLOCK/4 (clock C**8**) clocks the logic ones into flipflops **48**, **56** and **60** and sets their Q-outputs to logic one. The OCTANT signal switches to "010" and no longer matches the OCTANT SELECT signal. The COMPARE signal returns to logic zero. XOR gate **50** receives a logic zero from the $\overline{Q}$-output of flipflop **48** and a logic one from the Q-output of flipflop **56** and sets the second input of OR gate **44** to logic one. The D-input of flipflop **56** receives a logic one from OR gate **44**. AND gate **52** receives logic zeroes from flipflops **48** and **56**. XOR gate **58** receives a logic zero from AND gate **52** and a logic one from flipflop **60** and provides a logic one to OR gate **46**. The D-input of flipflop **60** goes to logic one.

The fourth rising edge of CLOCK/4 (clock C**12**) sets the $\overline{Q}$-output of flipflop **48** to logic one while the Q-outputs of flipflops **56** and **60** remain logic one. The output of OR gate **42** goes to logic one. XOR gate **50** receives a logic one from the $\overline{Q}$-output of flipflop **48** and a logic one from the Q-output of flipflop **56** and sets the second input of OR gate **44** to logic zero. The D-input of flipflop **56** receives a logic zero from OR gate **44**. AND gate **52** receives a logic one from flipflop **48** and a logic zero from flipflop **56**. XOR gate **58** receives a logic zero from AND gate **52** and a logic one from flipflop **60** and provides a logic one to OR gate **46**. The D-input of flipflop **60** goes to logic one.

The fifth rising edge of CLOCK/4 (clock C**16**) sets the Q-outputs of flipflops **48** and **60** to logic one while the Q-output of flipflop **56** goes to logic zero. The output of OR gate **42** goes to logic zero. XOR gate **50** receives logic zeroes from the $\overline{Q}$-output of flipflop **48** and the Q-output of

flipflop **56** and sets the second input of OR gate **44** to logic zero. The D-input of flipflop **56** receives a logic zero from OR gate **44**. AND gate **52** receives a logic zero from flipflop **48** and a logic one from flipflop **56**. XOR gate **58** receives a logic zero from AND gate **52** and a logic one from flipflop **60** and provides a logic one to OR gate **46**. The D-input of flipflop **60** goes to logic one.

The sixth rising edge of CLOCK/4 (clock C**20**) sets the $\overline{Q}$-outputs of flipflops **48** and **56** to logic one while the Q-output of flipflop **60** remains logic one. XOR gate **50** receives a logic one from the $\overline{Q}$-output of flipflop **48** and a logic zero from the Q-output of flipflop **56** and sets the second input of OR gate **44** to logic one. The D-input of flipflop **56** receives a logic one from OR gate **44**. AND gate **52** receives logic ones from flipflops **48** and flipflop **56**. XOR gate **58** receives a logic one from AND gate **52** and a logic one from flipflop **60** and provides a logic zero to OR gate **46**. The D-input of flipflop **60** goes to logic zero.

The seventh rising edge of CLOCK/4 (clock C**24**) sets the TRANSFER DATA signal to logic zero. The TRANSFER DATA signal remains logic zero for the next four CLOCK/4 cycles, i.e. C**24**–C**31** and C**0**–C**7**, as the down counter completes the second half of its count down sequence. Logic **40** thus provides a symmetric 50% duty cycle. Either edge of the TRANSFER DATA signal may be used to trigger the external logic to send more data to parallel-serial converter **10**. By controlling the phase of TRANSFER DATA, the correct timing is established for data transfer so that the requested data arrives at the optimum time to maximize the operating speed of parallel-serial converter **10**.

The aforedescribed phase control over the TRANSFER DATA is equally applicable to serial-parallel conversion such as shown in FIG. **3**. Serial-parallel converter **70** is shown suitable for manufacturing as an integrated circuit using conventional integrated circuit processes. The data input of flipflop **72** receives the serial DATA IN signal from external sourcing logic (not shown) and passes it to multiplexer **74** at each FLIPFLOP CLOCK. Multiplexer **74** rotates through its individual bit locations under control of the MUX ADDRESS signal and provides parallel bits to register **76**. Register **76** loads data at rising edge of a REGISTER CLOCK signal. A CMOS-ECL voltage translator circuit **78** converts the 32-bit data word from register **76** to CMOS logic levels.

Timing logic **80** operates in response to a SYSTEM CLOCK signal, operating for example at 2.5 gigahertz, for providing the FLIPFLOP CLOCK signal and the REGISTER CLOCK signal. The FLIPFLOP CLOCK signal operates in phase and at the same frequency as the SYSTEM CLOCK. The REGISTER CLOCK signal are derived from dividing the SYSTEM CLOCK by value thirty-two. The REGISTER CLOCK signal is aligned on the same rising edge as the SYSTEM CLOCK. The MUX ADDRESS is reset to zero with each REGISTER CLOCK and counts up with the SYSTEM CLOCK to value thirty-two. Thus, the serialized data stream DATA OUT is sent at the SYSTEM CLOCK frequency with the duration of each serial bit time the same as the period of the SYSTEM CLOCK. Timing logic **20** further provides a CLOCK/4 signal and a 3-bit OCTANT signal. The CLOCK/4 signal is derived by dividing the SYSTEM CLOCK by value four aligned with the rising edges of SYSTEM CLOCK. The OCTANT signal takes one of eight binary encoded values (0 through 7) as seen in Table 1. Timing logic **80** includes combinational logic to divide the SYSTEM CLOCK and reset the MUX ADDRESS signal. Such combinational logic can be implemented from the aforedescribed operations.

Phase delay logic circuit **82** receives CLOCK/4 and OCTANT signals from timing logic **80**, and an OCTANT SELECT signal from external logic (not shown). ECL-CMOS translator **84** converts the TRANSFER DATA signal from phase delay logic circuit **82** to CMOS logic levels for the external logic. Upon receiving the WRITE control signal, the external logic sends the next DATA IN bit. Phase delay logic circuit **82** follows the same description given in FIG. **2** and asserts the TRANSFER DATA signal at the correct time to allow maximum operating speed for serial-parallel converter **70** given the required set-up and hold-time of register **76**.

By now it should be appreciated that the present invention provides proper timing of the data transfer between external data sourcing or sinking logic and data conversion circuits. Phase delay logic sets the delay for a transfer data control signal as programmed by a select signal. During a calibration sequence, the select signal is set to various values to determine proper delay time necessary before requesting that more data be read or written. Once the proper delay is determined by experimentation, the phase delay logic circuit asserts the transfer data signal at the correct time by controlling its phase, to allow maximum operating speed for the data conversion given the required set-up and hold-time of the embedded register and of the external logic. By controlling the phase of transfer data requests, the correct timing is established to ensure proper data set-up and hold times and to allow complete processing before the next data word needs to be read or written.

While specific embodiments of the present invention have been shown and described, further modifications and improvements will occur to those skilled in the art. It is understood that the invention is not limited to the particular forms shown and it is intended for the appended claims to cover all modifications which do not depart from the spirit and scope of this invention. The present invention is applicable to other types of data processing circuits that must control timing of incoming data.

What is claimed is:

1. A phase delay circuit, comprising:

a comparator having first and second inputs and an output, said first input receiving a first control signal, said second input receiving a second control signal, said output providing a compare signal having a first state when said first and second control signals match; and

a down counter responsive to said compare signal for initializing a count value and responsive to a clock signal for counting down to generate an output signal having a symmetric duty cycle.

2. The circuit of claim **1** wherein said down counter includes:

a first OR gate having first and second inputs and an output, said first input being coupled for receiving said compare signal; and

a first flipflop having a data input, a clock input, and an inverted output, said data input being coupled to said output of said first OR gate, said inverted output being coupled to said second input of said first OR gate, said clock input being coupled for receiving said clock signal.

3. The circuit of claim **2** wherein said down counter further includes:

a first exclusive-OR gate having first and second inputs and an output, said first input being coupled to said inverted output of said first flipflop;

a second OR gate having first and second inputs and an output, said first input being coupled for receiving said

compare signal, said second input being coupled to said output of said first exclusive-OR gate; and

a second flipflop having a data input, a clock input, and first and second complementary outputs, said data input being coupled to said output of said second OR gate, said first complementary output being coupled to said second input of said first exclusive-OR gate, said clock input being coupled for receiving said clock signal.

4. The circuit of claim 3 wherein said down counter further includes:

a first AND gate having first and second inputs and an output, said first input being coupled to said inverted output of said first flipflop, said second input being coupled to said second complementary output of said second flipflop;

a second exclusive-OR gate having first and second inputs and an output, said first input being coupled to said output of said first AND gate;

a third OR gate having first and second inputs and an output, said first input being coupled for receiving said compare signal, said second input being coupled to said output of said second exclusive-OR gate; and

a third flipflop having a data input, a clock input, and an output, said data input being coupled to said output of said third OR gate, said output being coupled to said second input of said second exclusive-OR gate and providing said output signal of said down counter, said clock input being coupled for receiving said clock signal.

5. The circuit of claim 4 wherein said comparator includes:

a third exclusive-OR gate having first and second inputs and an output, said first input being coupled for receiving a first bit of said first control signal, said second input being coupled for receiving a first bit of said second control signal;

a fourth exclusive-OR gate having first and second inputs and an output, said first input being coupled for receiving a second bit of said first control signal, said second input being coupled for receiving a second bit of said second control signal; and

a second AND gate having first and second inputs and an output, said first input being coupled to said output of said third exclusive-OR gate, said second input being coupled to said output of said fourth exclusive-OR gate, said output providing said compare signal.

6. The circuit of claim 5 wherein said comparator further includes a fifth exclusive-OR gate having first and second inputs and an output, said first input being coupled for receiving a third bit of said first control signal, said second input being coupled for receiving a third bit of said second control signal, said output being coupled to a third input of said second AND gate.

7. A method of selecting phase delay of a transfer data control signal, comprising the steps of:

comparing first and second control signals and generating a compare signal having a first state when said first and second control signals match; and

initializing a count value in response to said compare signal; and

counting down said count value in response to a clock signal to provide a most significant bit of said count value with a symmetric duty cycle.

8. A data conversion circuit, comprising:

a register having an input coupled for receiving parallel input data and having an output;

a multiplexer having an input coupled to said output of said register for providing serial data;

a comparator having first and second inputs and an output, said first input receiving a first control signal, said second input receiving a second control signal, said output providing a compare signal having a first state when said first and second control signals match; and

a down counter responsive to said compare signal for initializing a count value and responsive to a clock signal for counting down to generate a transfer data signal having a symmetric duty cycle to enable transfer of said parallel input data to said register.

9. The circuit of claim 8 wherein said down counter includes:

a first OR gate having first and second inputs and an output, said first input being coupled for receiving said compare signal; and

a first flipflop having a data input, a clock input, and an inverted output, said data input being coupled to said output of said first OR gate, said inverted output being coupled to said second input of said first OR gate, said clock input being coupled for receiving said clock signal.

10. The circuit of claim 9 wherein said down counter further includes:

a first exclusive-OR gate having first and second inputs and an output, said first input being coupled to said inverted output of said first flipflop;

a second OR gate having first and second inputs and an output, said first input being coupled for receiving said compare signal, said second input being coupled to said output of said first exclusive-OR gate; and

a second flipflop having a data input, a clock input, and first and second complementary outputs, said data input being coupled to said output of said second OR gate, said first complementary output being coupled to said second input of said first exclusive-OR gate, said clock input being coupled for receiving said clock signal.

11. The circuit of claim 10 wherein said down counter further includes:

a first AND gate having first and second inputs and an output, said first input being coupled to said inverted output of said first flipflop, said second input being coupled to said second complementary output of said second flipflop;

a second exclusive-OR gate having first and second inputs and an output, said first input being coupled to said output of said first AND gate;

a third OR gate having first and second inputs and an output, said first input being coupled for receiving said compare signal, said second input being coupled to said output of said second exclusive-OR gate; and

a third flipflop having a data input, a clock input, and an output, said data input being coupled to said output of said third OR gate, said output being coupled to said second input of said second exclusive-OR gate and providing said output signal of said down counter, said clock input being coupled for receiving said clock signal.

12. The circuit of claim 11 wherein said comparator includes:

a third exclusive-OR gate having first and second inputs and an output, said first input being coupled for receiving a first bit of said first control signal, said second input being coupled for receiving a first bit of said second control signal;

a fourth exclusive-OR gate having first and second inputs and an output, said first input being coupled for receiving a second bit of said first control signal, said second input being coupled for receiving a second bit of said second control signal; and

a second AND gate having first and second inputs and an output, said first input being coupled to said output of said third exclusive-OR gate, said second input being coupled to said output of said fourth exclusive-OR gate, said output providing said compare signal.

13. The circuit of claim 12 wherein said comparator further includes a fifth exclusive-OR gate having first and second inputs and an output, said first input being coupled for receiving a third bit of said first control signal, said second input being coupled for receiving a third bit of said second control signal, said output being coupled to a third input of said second AND gate.

14. A data conversion circuit, comprising:

a multiplexer having an input coupled for receiving serial input data and having an output;

a register having an input coupled to said output of said register for providing prarllel data;

a comparator having first and second inputs and an output, said first input receiving a first control signal, said second input receiving a second control signal, said output providing a compare signal having a first state when said first and second control signals match; and

a down counter responsive to said compare signal for initializing a count value and responsive to a clock signal having a symmetric duty cycle to enable transfer of said serial input data to said register.

15. The circuit of claim 14 wherein said down counter includes:

a first OR gate having first and second inputs and an output, said first input being coupled for receiving said compare signal; and

a first flipflop having a data input, a clock input, and an inverted output, said data input being coupled to said output of said first OR gate, said inverted output being coupled to said second input of said first OR gate, said clock input being coupled for receiving said clock signal.

16. The circuit of claim 15 wherein said down counter further includes:

a first exclusive-OR gate having first and second inputs and an output, said first input being coupled to said inverted output of said first flipflop;

a second OR gate having first and second inputs and an output, said first input being coupled for receiving said compare signal, said second input being coupled to said output of said first exclusive-OR gate; and

a second flipflop having a data input, a clock input, and first and second complementary outputs, said data input being coupled to said output of said second OR gate, said first complementary output being coupled to said second input of said first exclusive-OR gate, said clock input being coupled for receiving said clock signal.

17. The circuit of claim 161wherein said down counter further includes:

a first AND gate having first and second inputs and an output, said first input being coupled to said inverted output of said first flipflop, said second input being coupled to said second complementary output of said second flipflop;

a second exclusive-OR gate having first and second inputs and an output, said first input being coupled to said output of said first AND gate;

a third OR gate having first and second inputs and an output, said first input being coupled for receiving said compare signal, said second input being coupled to said output of said second exclusive-OR gate; and

a third flipflop having a data input, a clock input, and an output, said data input being coupled to said output of said third OR gate, said output being coupled to said second input of said second exclusive-OR gate and providing said output signal of said down counter, said clock input being coupled for receiving said clock signal.

18. The circuit of claim 17 wherein said comparator includes:

a third exclusive-OR gate having first and second inputs and an output, said first input being coupled for receiving a first bit of said first control signal, said second input being coupled for receiving a first bit of said second control signal;

a fourth exclusive-OR gate having first and second inputs and an output, said first input being coupled for receiving a second bit of said first control signal, said second input being coupled for receiving a second bit of said second control signal; and

a second AND gate having first and second inputs and an output, said first input being coupled to said output of said third exclusive-OR gate, said second input being coupled to said output of said fourth exclusive-OR gate, said output providing said compare signal.

19. The circuit of claim 18 wherein said comparator further includes a fifth exclusive-OR gate having first and second inputs and an output, said first input being coupled for receiving a third bit of said first control signal, said second input being coupled for receiving a third bit of said second control signal, said output being coupled to a third input of said second AND gate.

* * * * *

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 5,563,594
DATED : October 8, 1996
INVENTOR(S) : David K. Ford et al.

It is certified that error appears in the above-indentified patent and that said Letters Patent is hereby corrected as shown below:

In claim 14, column 9, line 30, insert --for counting down to generate a transfer data signal-- after "signal".

In claim 17, column 10, line 7, delete "161wherein" and insert --16 wherein--.

Signed and Sealed this

Twenty-ninth Day of April, 1997

Attest:

Attesting Officer

BRUCE LEHMAN

Commissioner of Patents and Trademarks

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

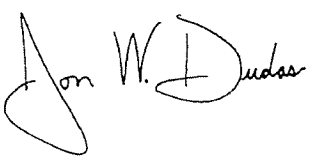
PATENT NO. : 5,563,594
DATED : October 8, 1996
INVENTOR(S) : David K. Ford and Bernard E. Weir, III

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Column 9,
Line 22, please change "prarllel" to -- parallel --.

Signed and Sealed this

Twenty-second Day of March, 2005



JON W. DUDAS
Director of the United States Patent and Trademark Office

EXHIBIT B

US006362644B1

(12) **United States Patent**
Jeffery et al.

(10) **Patent No.: US 6,362,644 B1**
(45) **Date of Patent: Mar. 26, 2002**

(54) **PROGRAMMABLE TERMINATION FOR INTEGRATED CIRCUITS**

(75) Inventors: **Philip A. Jeffery**, Tempe; **Stephen G. Shook**, Gilbert, both of AZ (US)

(73) Assignee: **Semiconductor Components Industries LLC**, Phoenix, AZ (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **09/630,090**

(22) Filed: **Aug. 1, 2000**

(51) **Int. Cl.**[7] **H03K 17/16**
(52) **U.S. Cl.** **326/30**; 326/101
(58) **Field of Search** 326/30, 62, 63, 326/101; 327/333, 564, 565

(56) **References Cited**

U.S. PATENT DOCUMENTS

5,341,039 A * 8/1994 Fukumoto 326/30
5,374,861 A * 12/1994 Kubista 326/30
5,731,711 A * 3/1998 Gabara 326/30
5,781,028 A * 7/1998 Decuir 326/30
6,114,898 A * 9/2000 Okayasu 327/437

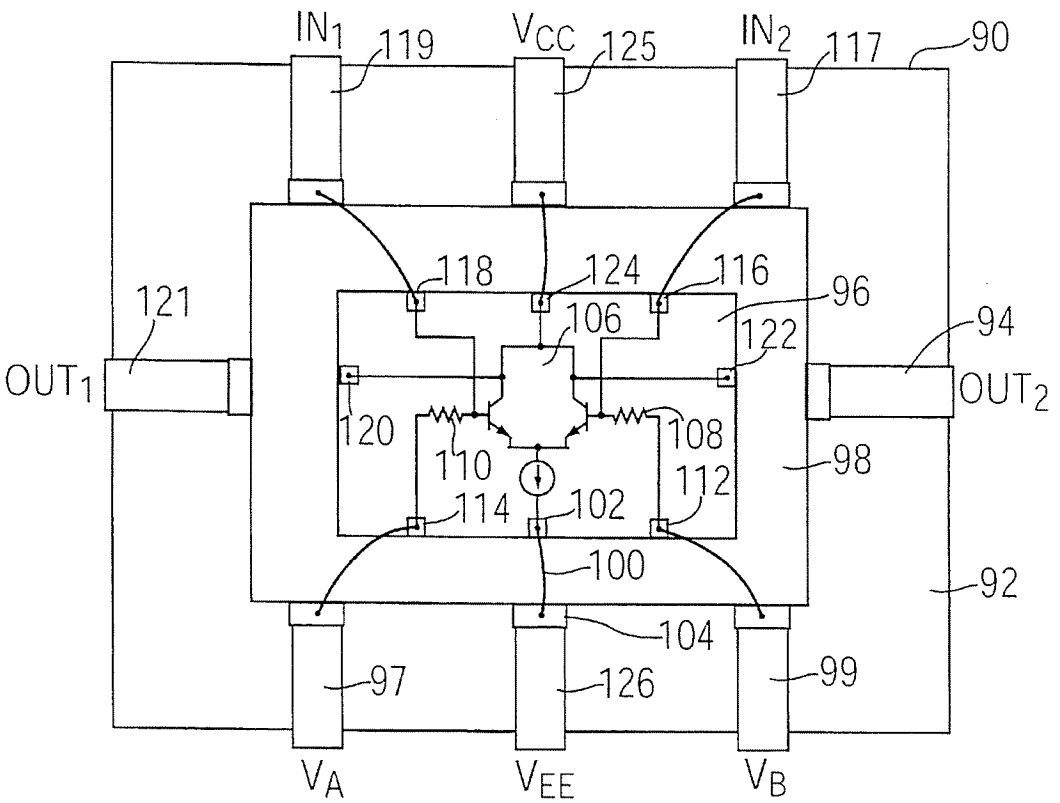
* cited by examiner

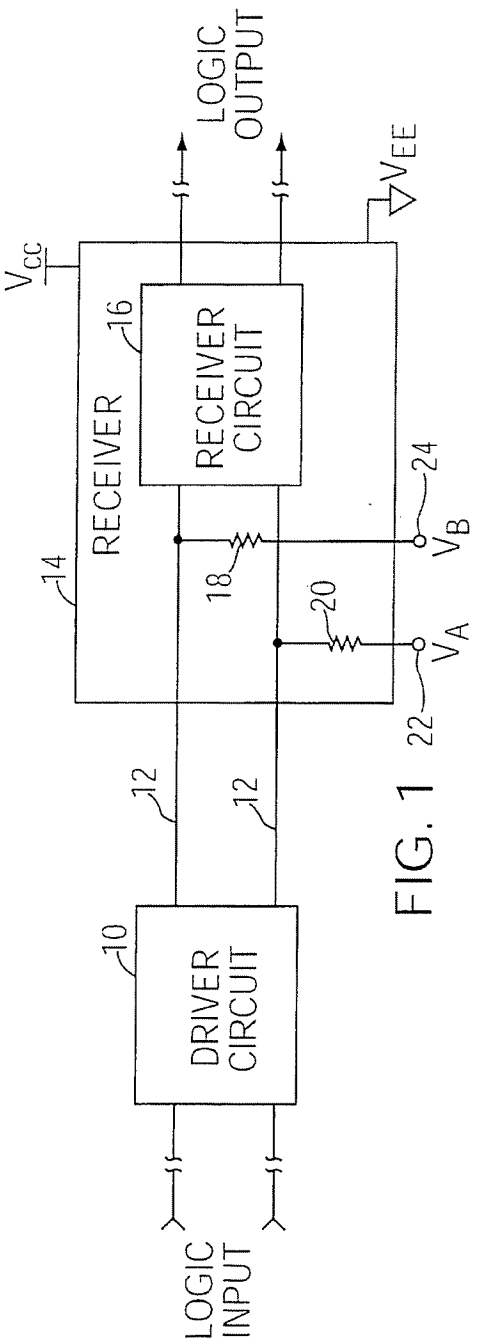
Primary Examiner—Tuan T. Lam

(57) **ABSTRACT**

A receiver circuit (**16**) is programmable to operate with different logic family driver circuits (**10**). The receiver circuit has two external configuration pins (**22**,) **24**) that are configured to provide the necessary termination for the type of logic family driver circuit used. To terminate the receiver circuit (**16**) for an ECL application will require first and second configuration pins (**22**,**24**) are connected to V_{CC}—2 volts. To terminate the receiver circuit (**16**) for a CML application will require the first configuration pin (**22**) and the second configuration pin (**24**) are connected to V_{CC}. LVDS termination for the receiver circuit (**16**) requires the first configuration pin (**22**) and the second configuration pin (**24**) are connected together. The configuration pins are external to a semiconductor package (**14**) housing the receiver circuit.

16 Claims, 3 Drawing Sheets

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RECEIVER
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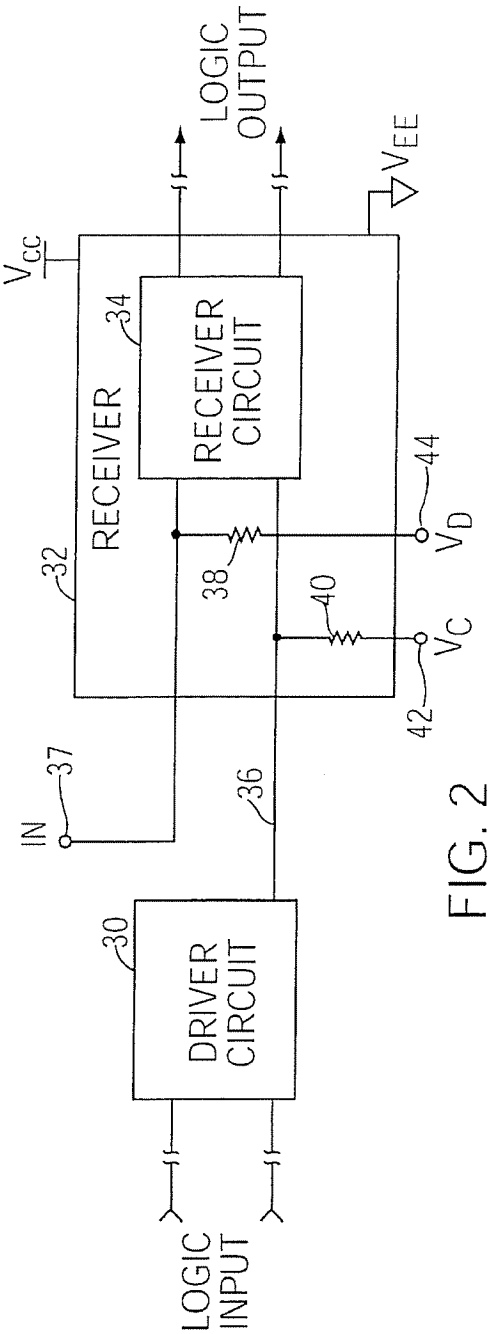
DRIVER CIRCUIT
LOGIC INPUT

FIG. 1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IN
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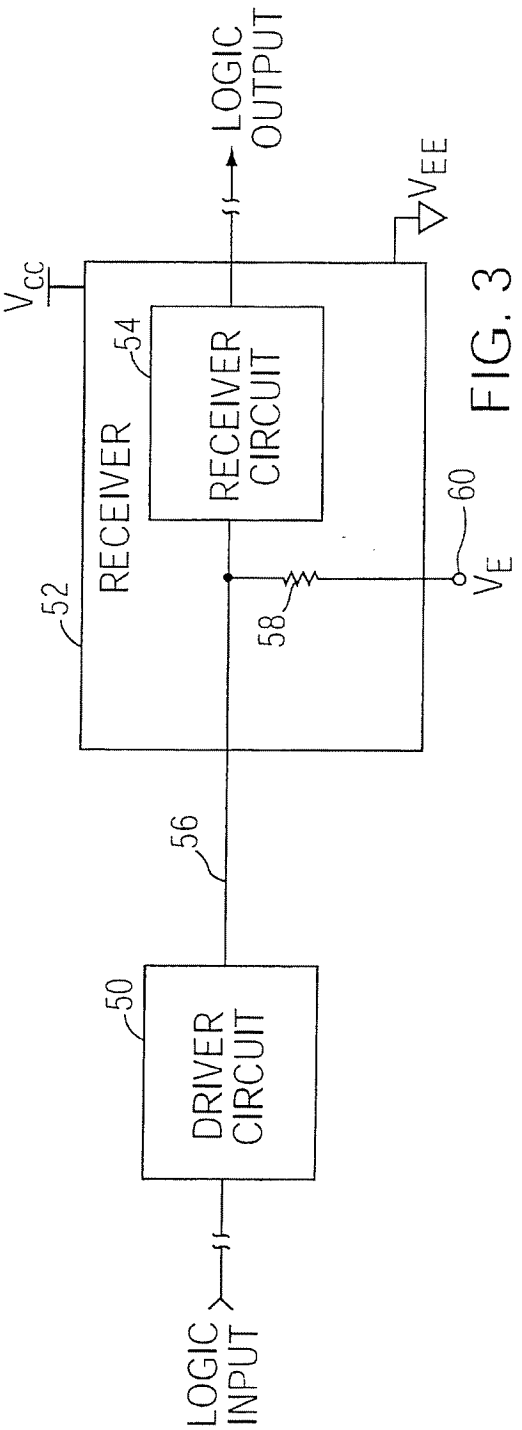
DRIVER CIRCUIT
LOGIC INPUT

FIG. 2


LOGIC OUTPUT
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58
56
50
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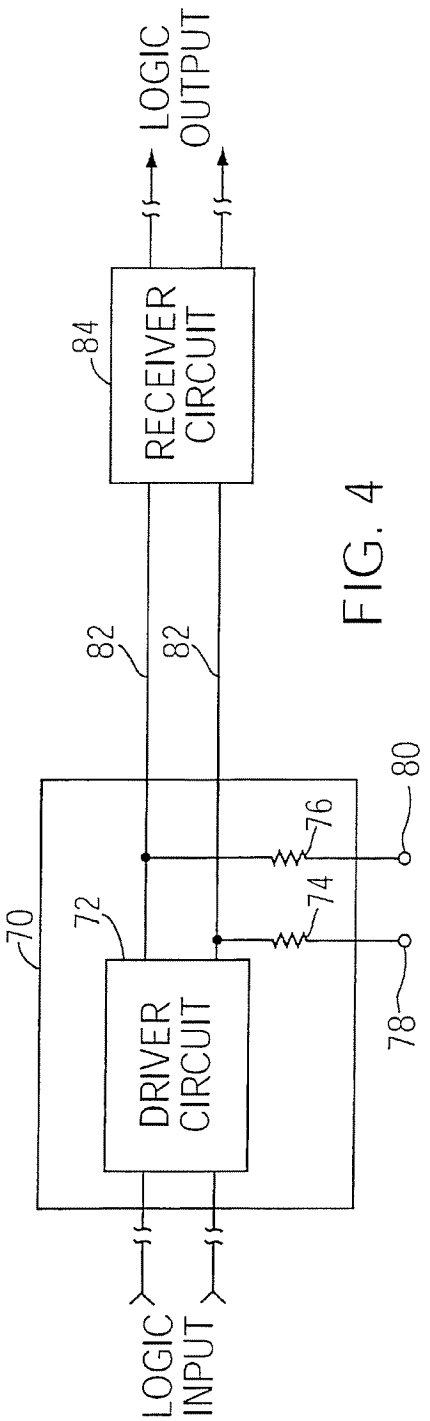
LOGIC INPUT

FIG. 3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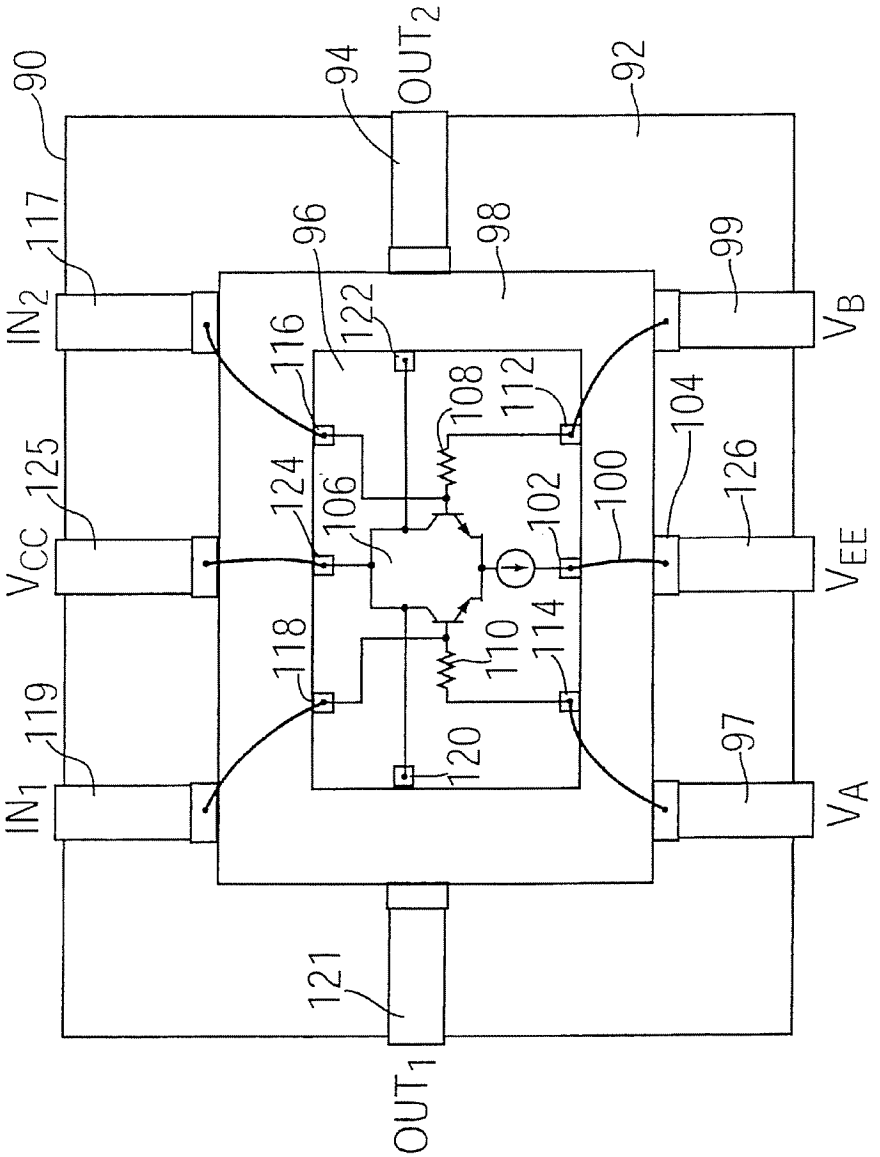
LOGIC INPUT

FIG. 4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119
IN1
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97
VA
121
OUT1

FIG. 5

PROGRAMMABLE TERMINATION FOR INTEGRATED CIRCUITS

BACKGROUND OF THE INVENTION

The present invention relates in general to electronic circuits and, more particularly, to logic circuits.

Many logic family applications have logic devices that operate within a mixed signal environment. The logic devices have logic drivers that may communicate with a logic receiver of a different logic family type. Typically, different logic family devices communicate with each other using translators to convert, for example, an ECL signal from the logic driver to a CMOS signal received at the logic receiver. A different type of translator is required for each type of logic driver and logic receiver used within the mixed signal environment. In addition, systems usually have an external termination scheme on an interconnect transmission line between the logic driver and logic receiver so the logic receiver circuit is terminated to receive the specific logic driver family type. The termination is a resistance that provides a termination for the logic device through to a voltage source Vtt. The voltage source Vtt is typically different for each logic family application. The resistance is typically chosen to equal the impedance of the interconnect transmission line to help reduce interconnect signal distortion. It is more of an advantage to have terminations as close as possible to the logic receiver circuit to help reduce interconnect signal distortion even more. Also, prior art termination schemes typically require different termination connections are used for each type of logic family device. For example, to use an ECL logic device requires a 50 ohm termination to a Vtt voltage source. A CML logic device may require termination through a resistance to a different voltage source. Most prior art logic family devices also have the termination resistors hard-wired to a circuit board making it difficult to change terminations for different logic family applications.

Hence, it is desired to have a logic receiver circuit that is programmable to allow the logic receiver circuit to communicate with different logic family driver circuits. Furthermore, it is desirable to have the terminations internal to the logic receiver circuit package so the terminations are close to the receiving circuit to help eliminate transmitted signal noise. The invention disclosed herein will address the above problems.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a schematic diagram of a driver and receiver circuit in a differential configuration;

FIG. **2** is a schematic diagram of a driver and receiver circuit in a single-ended configuration;

FIG. **3** is a schematic diagram of a driver and receiver circuit in a modified single-ended configuration;

FIG. **4** is a schematic diagram of a driver and receiver circuit in a differential configuration with driver circuit terminations; and

FIG. **5** is a schematic diagram of a receiver circuit showing semiconductor and package connections.

DETAILED DESCRIPTION OF THE PREFERED EMBODIMENT

FIG. **1** illustrates an embodiment of a driver circuit and a receiver circuit system used in a differential configuration. The differential configuration receives a logic input signal at driver circuit **10**. Driver circuit **10** is a device from a typical

logic family, e.g. ECL, CML, LVDS, CMOS, and TTL, or can be an analog driver circuit. The primary purpose of driver circuit **10** is to provide a signal boost for the logic input signal. At the output to driver circuit **10** is differential line **12** which transmits a differential signal from driver circuit **10** to receiver package **14**. Receiver package **14** is a semiconductor package housing receiver circuit **16**. V_{CC} and V_{EE} are power supply potentials to receiver package **14** providing power to receiver circuit **16**. Receiver circuit **16** receives a differential input signal on differential line **12** and provides a logic output signal. Receiver circuit **16** is typically a differential receiver circuit amplifier manufactured as a semiconductor die. Receiver circuit **16** and receiver package **14** are an integrated receiver circuit.

Differential line **12** is terminated with load element **18** and load element **20**. Load element **18** is connected to configuration pin **24** and load element **20** is connected to configuration pin **22**. Load elements **18**, **20** are resistors contained within receiver package **14** having a resistance of 50, 75, or 100 ohms. Configuration pins **22**, **24** are external pins connected to receiver package **14** and are programmable so receiver circuit **16** can communicate with different logic family drivers. To program configuration pins **22**, **24**, the pins are terminated using a configuration which is dependent on the desired logic family application. The configuration of receiver circuit **16** is controlled by connecting configuration pin **22** (V_A) and configuration pin **24** (V_B) as follows.

ECL:	$V_A = V_B = V_{cc} - 2$ volts
CML:	$V_A = V_B = V_{CC}$
LVDS:	V_A connected to V_B

For example, to terminate receiver circuit **16** for an ECL application requires configuration pin **22** (V_A) and configuration pin **24** (V_B) are connected to receive configuration signal, V_{CC}-2 volts. To terminate receiver circuit **16** for an CML application requires configuration pin **22** (V_A) and configuration pin **24** (V_B) are connected to to receive configuration signal, V_{CC}. LVDS termination for receiver circuit **16** requires configuration pin **22** (V_A) and configuration pin **24** (V_B) are connected together. Termination of the configuration pins **22**, **24** is done external to receiver package **14**.

FIG. **2** illustrates an embodiment of a driver circuit and a receiver circuit system used in a single-ended configuration. The single-ended configuration receives a logic input signal at driver circuit **30**. Driver circuit **30** is a device from a typical logic family, e.g. ECL, CML, LVDS, CMOS, and TTL, or can be an analog driver circuit. Driver circuit **30** provides a signal boost for the logic input signal. Line **36** is connected to the output of driver circuit **30** to transmit a signal from driver circuit **30** to receiver package **32**. Receiver package **32** is a semiconductor package for receiver circuit **34**. V_{CC} and V_{EE} are power supply potentials to receiver package **32** providing power to receiver circuit **34**. Receiver circuit **30** is typically a differential receiver circuit amplifier manufactured as a semiconductor die. Receiver circuit **30** and receiver package **32** are an integrated receiver circuit.

Receiver circuit **34** receives two input signals: an information signal from driver circuit **30** on terminal **36**, and control signal IN on terminal **37**. Receiver circuit **34** is terminated at terminal **36** with load element **40**, and at terminal **37** with load element **38**. Load element **38** is connected to configuration pin **44** and load element **40** is connected to configuration pin **42**. Load elements **38**, **40** are

resistors contained within receiver package **32** having a resistance of 50, 75, or 100 ohms. Configuration pins **42**, **44** are external pins connected to receiver package **32** and are programmable so receiver circuit **34** can communicate with different logic family drivers. Configuration pins **42**, **44** are programmed by terminating the pins using a configuration which is dependent on the desired logic family application. The configuration of receiver circuit **34** is controlled by connecting configuration pin **42** (V_C) and configuration pin **44** (V_D) as follows.

ECL:	$V_C = V_{CC} - 2$ volts
	V_D = open
	IN = V_{BB}
CMOS:	V_C = open
	V_D = open
	IN = $V_{CC}/2$
TTL:	V_C = open
	V_D = open
	IN = 1.5 volts

V_{BB} is typically the middle of an output swing to an ECL output. To terminate receiver circuit **34** for an ECL application requires configuration pin **42** (V_C) is connected to receive configuration signal, $V_{CC}-2$, configuration pin **44** (V_D) is devoid of a configuration signal, i.e. is left open, and terminal **37** is connected to receive control signal, V_{BB}. To terminate receiver circuit **34** for a CMOS application requires configuration pin **42** (V_C) and configuration pin **44** (V_D) are devoid of a configuration signal, and terminal **37** is connected to receive control signal, $V_{CC}/2$. TTL termination for receiver circuit **34** requires configuration pin **42** (V_C) and configuration pin **44** (V_D) are devoid of a configuration signal, and terminal **37** is connected to receive control signal, 1.5 volts. Termination of the configuration pins **42**, **44** is done external to receiver package **32**.

FIG. **3** illustrates an embodiment of a driver circuit and a receiver circuit system used in a modified single-ended configuration. The single-ended configuration receives a logic input signal at driver circuit **50**. Driver circuit **50** is a device from a typical type of logic family, e.g. ECL, CML, LVDS, CMOS, and TTL, or can be an analog driver circuit. Driver circuit **50** provides a signal boost for the logic input signal. Receiver package **52** receives a drive signal on line **56** from driver circuit **50**. Receiver package **52** is a semiconductor package for receiver circuit **54**. V_{CC} and V_{EE} are power supply potentials to receiver package **52** providing power to receiver circuit **54**. Receiver circuit **54** is terminated with load element **58** which is connected to configuration pin **60**. Load element **58** is a resistor contained within receiver package **52** having a resistance of 50, 75, or 100 ohms. Configuration pin **60** is an external pin connected to receiver package **52** that is programmable so receiver circuit **54** can communicate with different logic family drivers. Configuration pin **60** is programmed by terminating the pin using a configuration which is dependent on the desired logic family application. The configuration of receiver circuit **54** is controlled by connecting configuration pin **60** (V_E) as follows.

ECL:	$V_E = V_{CC} - 2$
CML:	$V_E = V_{CC}$
LVDS:	V_E = open

To terminate receiver circuit **54** for an ECL application requires that configuration pin **60** (V_E) is connected to receive configuration signal, $V_{CC}-2$. For a CML application, receiver circuit **54** is terminated with configuration pin **60** (V_E) connected to receive configuration signal, V_{CC}. LVDS termination for receiver circuit **54** requires that configuration pin **60** (V_E) be left open. Termination of the configuration pin **60** is done external to receiver package **52**.

FIG. **4** illustrates a differential configuration similar to FIG. **1**, except termination is done on driver package **70**. Driver circuit **72** is terminated at load element **74** and load element **76**. Load element **74**, **76** are resistors contained within driver package **70** having a value of 50, 75, or 100 ohms. Configuration pin **78** and configuration pin **80** are configured similar to table shown for the differential configuration in FIG. **1**. Driver circuit **72** provides an output signal on differential line **82** to receiver circuit **84**.

FIG. **5** illustrates a detailed schematic of the differential configuration in FIG. **1**. Semiconductor package **90** houses a leadframe **92** with metal leads similar to lead **94** which provide input and output signals. The input and output signals consist of differential input logic signals IN_1, and IN_2, differential output logic signals OUT_1, and OUT_2, power supply signals V_{CC} and V_{EE}, and configuration signals V_A and V_B on configuration pins **97**, **99** respectfully. Semiconductor die **96** is attached to flag **98** which is attached to leadframe **92**. Bond wire **100** is attached to bond pad **102** on semiconductor die **96** to provide electrical contact to bond pad **104** for the V_{EE} signal. All other input and output signals have the same bond wire configuration to provide electrical contact. The wire bonding technology used is typically a bump type technology or a ball grid array (BGA) technology. The differential configuration typically has differential amplifier **106** for receiver circuit **16** of FIG. **1**. Load elements **108**, **110** are connected to bond pads **112**, **114** respectfully to provide an electrical connection to configuration signals V_B and V_A. The differential signal from logic circuit **10** of FIG. **1** is received at lead **119** (IN_1) and lead **117** (IN_2) which has electrical contact to bond pads **118**, **116** on semiconductor die **96**, and to differential amplifier **106**. The logic output signal from receiver circuit **16** of FIG. **1** is coupled from differential amplifier **106**, electrical contact is made to bond pads **120**, **122** on semiconductor die **96**, and the signals are coupled to leads **121**. (OUT_1) and **94** (OUT_2) respectfully. Power supply is received at leads **125** (V_{CC}) and **126** (V_{EE}) making electrical contact to differential amplifier **106** through bond pads **124**, **102** respectively.

An alternative method to provide termination to any of the above embodiments is to use a switch between the termination (load) elements and the (configuration) termination signals. For example, FIG. **1** has external (configuration) termination pins **22**, **24** which are configured to receive different termination signals depending on the logic family application. A switch can be used to programmably connect termination pins **22**, **24** to $V_{CC}-2$ for an ECL logic family application, or to V_{CC} for a CML logic family application. The switch can provide programmability for the termination signals to any of the previous configurations outlined herein.

Thus, a technique for generating multiple input termination options on a single integrated circuit is disclosed. A receiver circuit is programmable to configure different termination connections which allow the receiver circuit to communicate with a driver circuit from a different logic family. The receiver circuit has at least one external configuration pin that is configured to provide the necessary termination for the type of logic family driver circuit used. The configuration pin is external to a semiconductor package housing the receiver circuit. Having configuration pins external to the semiconductor package provides for easy

portability among different logic families, and easy termination options which require no additional translators to operate a mixed logic family system.

What is claimed is:

1. An integrated logic circuit having a differential input receiving a differential signal, comprising:

a receiver having first and second inputs coupled for receiving the differential signal;

a semiconductor package for housing the receiver, having first and second pins respectively coupled to the first and second inputs of the receiver, and a supply pin coupled to the receiver for providing a power supply potential;

a first termination element housed in the semiconductor package and coupled between the first input of the receiver and a first programmable configuration pin of the semiconductor package; and

a second termination element housed in the semiconductor package and coupled between the second input of the receiver and a second programmable configuration pin of the semiconductor package, wherein the first and second programmable configuration pins receive first and second termination signals to configure termination for the logic circuit.

2. The integrated logic circuit of claim 1, wherein the first and second termination elements comprise resistors.

3. A method of configuring a receiver circuit using first and second configuration signals, and receiving first and second input signals to the receiver circuit, comprising:

coupling an information signal on the first input to the receiver circuit;

coupling a control signal on the second input to the receiver circuit;

providing a first programmable configuration pin of a semiconductor package housing the receiver circuit;

connecting a first load element between the first input of the receiver circuit and the first programmable configuration pin;

providing a second programmable configuration pin of a semiconductor package housing the receiver circuit; and

connecting a second load element between the second input of the receiver circuit and the second programmable configuration pin.

4. The method of claim 3, wherein the first and second programmable configuration pins receive a configuration selected from the group consisting of the first configuration signal, the second configuration signal, and devoid of the first and second configuration signals.

5. The method of claim 3, wherein the second input receives a control signal selected from the group consisting of a first control signal, a second control signal, and a third control signal.

6. An integrated circuit, comprising:

a semiconductor package having first and second pins respectively adapted for receiving first and second data signals, third and fourth pins for respectively receiving first and second termination signals, and a supply pin coupled for receiving a power supply voltage; and

a semiconductor die housed in the semiconductor package for operating from the power supply voltage, and having a first load element coupled between the first and third pins to terminate the first data signal, and a second load element coupled between the second and fourth pins to terminate the second data signal.

7. The integrated circuit of claims 6, wherein the first and second load elements are resistors.

8. The integrated circuit of claim 6, wherein the semiconductor die includes a receiver circuit having first and second inputs coupled to the first and second pins, respectively.

9. The integrated circuit of claim 6, wherein the semiconductor die includes a driver circuit having first and second outputs coupled to the first and second pins, respectively.

10. The integrated circuit of claim 6, wherein the first data signal is from a first logic family, and the third pin is coupled for receiving a first termination voltage characteristic of the first logic family.

11. The integrated circuit of claim 10, wherein the second data signal is from a second logic family, and the fourth pin receives a second termination voltage of the second logic family.

12. A method of operating an integrated circuit, comprising the steps of:

applying first and second logic signals to first and second pins, respectively, of a semiconductor package of the integrated circuit; and

loading the first and second logic signals with first and second load elements, respectively, of the integrated circuit, where the first and second load elements are coupled to third and fourth pins of the semiconductor package to provide a programmable termination for the first and second logic signals.

13. The method of claim 12, wherein the first and second logic signals function as a differential signal and the third and fourth pins are for coupling together to terminate the differential signal.

14. The method of claim 12, wherein the first and second logic signals are specified in accordance with first and second logic families and the third and fourth pins are coupled to first and second configuration signals of the first and second logic families, respectively.

15. The method of claims 14, wherein the first and second logic signals are ECL signals referenced to a supply voltage, and the first and second configuration signals have values equal to the supply voltage minus about two volts.

16. The integrated logic circuit of claim 12, further comprising the step of applying a power supply voltage to a fifth pin of the semiconductor package to bias the integrated circuit.

* * * * *

EXHIBIT C

US005361001A

United States Patent [19]

Stolfa

[11] Patent Number: 5,361,001

[45] Date of Patent: Nov. 1, 1994

[54] CIRCUIT AND METHOD OF PREVIEWING ANALOG TRIMMING

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[73] Assignee: Motorola, Inc., Schaumburg, Ill.

[21] Appl. No.: 160,762

[22] Filed: Dec. 3, 1993

[51] Int. Cl.[5] H03K 3/01; H03B 1/04

[52] U.S. Cl. 327/530; 327/525; 327/312

[58] Field of Search 307/202.1, 296.1, 547, 307/548

[56] References Cited

U.S. PATENT DOCUMENTS

4,158,786 6/1979 Hirasawa 307/296.1
4,446,534 5/1984 Smith 307/202.1

FOREIGN PATENT DOCUMENTS

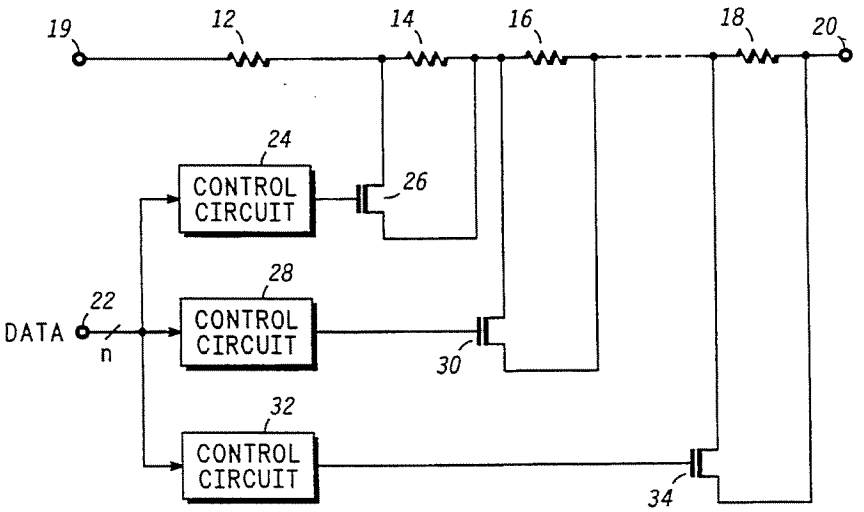
0112298 5/1987 Japan 307/202.1
0262716 10/1990 Japan 307/202.1

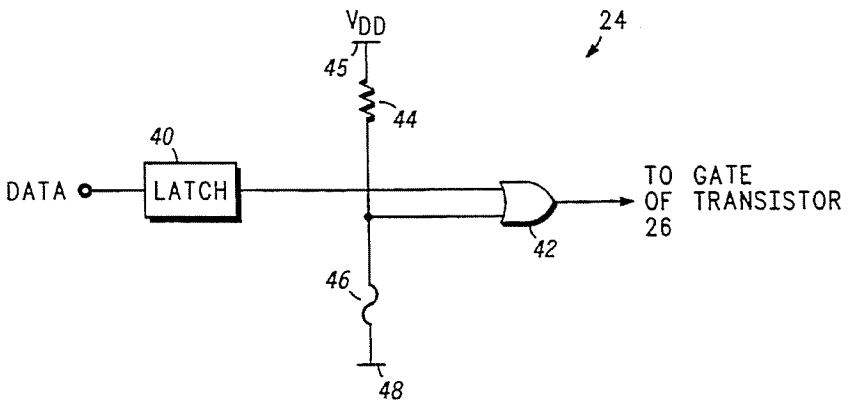
Primary Examiner—Margaret Rose Wambach
Attorney, Agent, or Firm—Robert D. Atkins

[57] ABSTRACT

An analog trim circuit enables and disables one or more serially connected passive elements for setting characteristics of the circuit. Each passive element has a transistor across its first and second conduction terminals operating in response to a control signal from a control circuit for enabling and disabling conduction through the associated passive element. The control circuits are responsive to a data signal for providing the control signals that enable and disable the conduction through the passive elements. The data signal allows a preview of the trimming results. The fuse in certain ones of the control circuits are blown to set the control signals to fixed values after removal of the data signal.

7 Claims, 1 Drawing Sheet





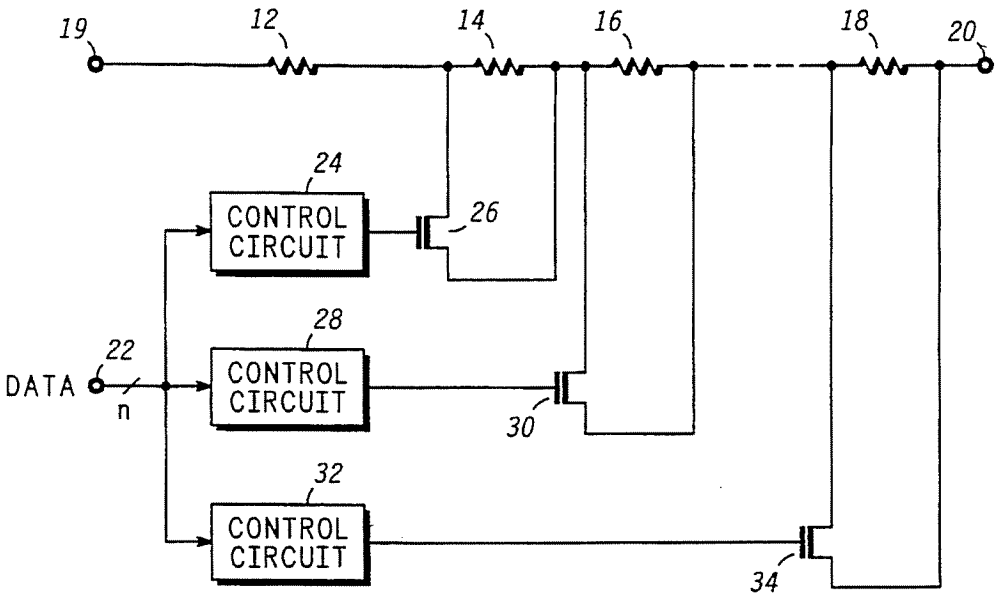
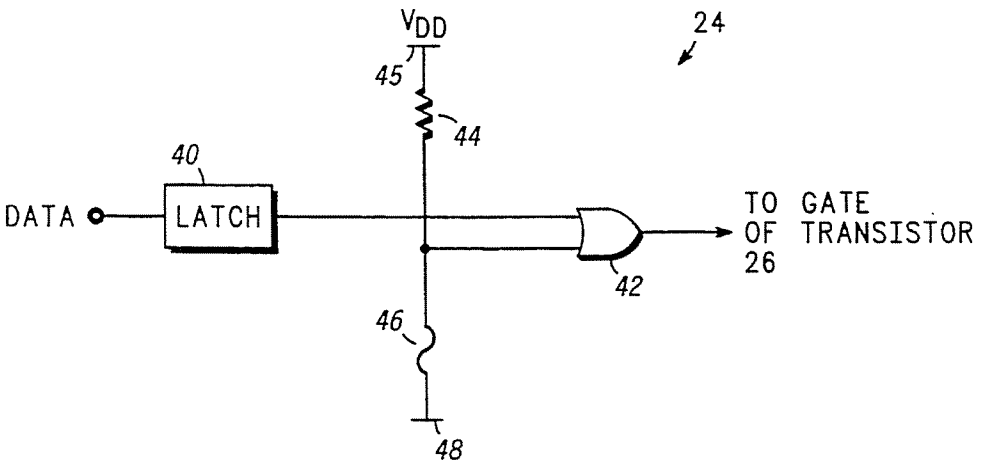

19
12
14
16
18
20
24
CONTROL CIRCUIT
26
28
CONTROL CIRCUIT
22
DATA
n
30
32
CONTROL CIRCUIT
34
10

FIG. 1

FIG. 2


V_{DD}
45
24
44
40
DATA
LATCH
TO GATE OF TRANSISTOR 26
42
46
48

CIRCUIT AND METHOD OF PREVIEWING ANALOG TRIMMING

BACKGROUND OF THE INVENTION

The present invention relates in general to analog trim circuits and, more particularly, to a technique of previewing the analog trim results before blowing a fuse to lock the trim in place.

In manufacturing analog integrated circuits, the basic building blocks are usually not accurately controlled by the manufacturing process as may be desired. For example, capacitors and resistors may have the wrong value, and MOS transistors may have the wrong gain setting. There are too many variables in the manufacturing process to yield absolute predictable results. Yet historically analog circuits often require very accurate voltage references, frequency references, and accurately ratioed elements.

To compensate for the process variability, many electronic circuits use analog trimming during test to set resistor values as necessary for proper operation of the circuit. A typical trimming technique utilizes a resistor ladder comprising a series of serially coupled resistors each in parallel with either a fuse or anti-fuse. A fuse is a device that is substantially an electrical short until it is blown open. An anti-fuse is an electrical open until blown when it becomes substantially an electrical short.

The fuse-blowing approach may take several forms, each with its own shortcomings. Laser fuses may be used directly across each resistor element in the ladder to enable and disable conduction through the resistor. During test, certain resistors are selected to open the shunt element thereby adding resistance to the serial path. The resistor ladder should be adjustable at wafer test over a range from say 10 to 2,560 ohms in 10 ohm increments.

The analog trimming may be performed iteratively, i.e. test, trim, test, trim, to measure the effect of the course trim and determine the necessary fine trimming. For iterative trimming, a laser trim system is typically installed on the wafer tester to alternately test and trim. However, one laser system per tester is very expensive. The laser is often in an idle state waiting for the tester. Moreover, if either the test system or laser breaks down both are inoperative.

An alternate approach is to use a zener anti-fuse across the resistor ladder. Such an element can be cheaply trimmed on the tester so that iterative testing can be done in one pass on the tester. Zener anti-fuses require large currents to program. Therefore, each anti-fuse requires its own external pad and probe card needle. This restricts the programming bit count to say 5–10 bits before the die area for test pads and complexity of the probe card requirements become prohibitive.

In general, iterative testing is a slow and expensive process. Consequently, many trimming techniques utilize only a single pass to evaluate which resistors in the serial string should be included to achieve the desired analog circuit operation. Thus, as result of a test measurement, the user blows the shunt fuse elements whereby the circuit is expected to operate as planned. The process of blowing the fuses typically involves laser trimming off-line from the test set to cut the poly material and open the shunt element. The circuit may be returned to the test set to verify proper trimming. If the subsequent testing should fail, the part is typically discarded since it is difficult to patch the shunt fuse elements.

Hence, a need exists for an iterative trimming to evaluate the results of test before permanently setting the trim.

BRIEF DESCRIPTION OF THE DRAWING

FIG. **1** is a block diagram illustrating an analog trimming circuit; and

FIG. **2** is a schematic diagram illustrating the control circuit of FIG. **1**.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

An analog trim circuit is shown in FIG. **1** including a passive ladder network **10** comprising resistors **12**, **14**, **16** and **18** serially coupled between terminal **19** and terminal **20**. Resistor **12** is non-trimmable and provides the minimum ladder resistance (R_{MIN}). Resistors **14–18** are selected in an exponential series, such as 1280, 640, 320, 160, 80, 40, 20, and 10 ohms. Resistors **14–18** are passive elements each with first and second conduction terminals. Other passive elements may also be used in the trim circuit. A data signal is applied at terminal **22**. One bit of the data signal is applied to each of control circuits **20**, **28** and **32**. An address signal selects the control circuit to latch one bit of the data signal.

Control circuit **24** provides a control signal to the gate of MOS transistor **26**. The drain and source of transistor **26** are coupled to first and second conduction terminals of resistor **14**. Likewise, control circuit **28** provides a control signal to the gate of MOS transistor **30** which has its drain and source coupled across resistor **16**. Control circuit **32** provides a control signal to the gate of MOS transistor **34**. The drain and source of transistor **34** are coupled across the first and second conduction terminals of resistor **18**. The effective resistance through resistor ladder **10** is thus temporarily set by transistors **26**, **30** and **34** selectively enabling and disabling conduction through resistors **14–18** upon receiving a high state or low state of control signals from control circuits **24**, **28** and **32**. With the above trimming scheme, the resistor ladder is controllable from R_{MIN} to $R_{MIN}+2{,}560$ ohms assuming eight trimmable resistors in 256 possible 10 ohm increments.

Turning to FIG. **2**, further detail of control circuit **24** is shown. Control circuits **28** and **32** follow a similar construction and operation as described for control circuit **24**. The data signal is latched in latching circuit **40** for application to a first input of OR gate **42**. An address signal enables latching circuit **40** to latch the data bit. Resistor **44** is coupled between the second input of OR gate **42** and power supply conductor **45**. Power supply conductor **45** operates at a positive potential VDD such as 5 volts. Fuse **46** is coupled between the second input of OR gate **42** and power supply conductor **48** operating at ground potential. The output of OR gate **42** provides the control signal to the gate of transistor **26**. An alternate embodiment of control circuit **24** may replace OR gate **42** with a NAND gate while resistor **44** and fuse **46** exchange places in the circuit.

Trim circuits are used in a variety of applications. For example, a circuit may require a given frequency f_o determined by an RC time constant such that the frequency is inversely proportional to RC. The resistance R and capacitance C should be selected such that the nominal process target values of sheet ρ (resistance per

unit area) and capacitance per unit area yield the desired frequency f_o. However, the actual process values of resistance and capacitance may vary by 5%–10%. Thus, the trimmable resistor ladder **10** must be trimmed to compensate for any variation in sheet ρ and capacitance per unit area.

During testing at wafer level, the circuit under test is exercised and any correction necessary to resistor ladder **10** is calculated by a binary search. Steps are taken to determine whether a resistor should be trimmed such that it is in the upper half or lower half of its trimmable range, i.e. determining if the most significant bit or largest resistor should be shorted or left to remain in resistor ladder **10**. With resistor ladder **10** trimmed to its most significant bit the circuit under test is again tested and a correction is calculated to determine if it should be trimmed to the upper half or lower half of the remaining trimmable range. As a result, the next most significant resistor is shorted or allowed to remain. The process continues until all trimmable resistors have been checked.

Consider the trimming operation during test where a logic one data signal is stored in latching circuit **40** of each of control circuits **24**, **28** and **32**. The output of each OR gate **42** goes high and enables transistors **26**, **30** and **34**. Resistors **14**–**18** are substantially shorted, i.e. disabling the conduction path through resistors **14**–**18**. The resistance of ladder **10** is equal to R_{MIN}.

To perform trim preview during test, the data signal to control circuit **24** is set to logic zero and stored in its latching circuit **40**. At wafer test all fuses are yet unblown so that all fuse inputs to the OR-gates are low. The control signal at the output of OR-gate **42** goes low and turns off transistor **26** to enable the conduction through resistor **14**. The resistance of ladder **10** increases to $R_{MIN}+R_{14}$, where R_{14} is the value of resistor **14**. The effect of the added resistance on the operation of the circuit under test may be checked and verified by the tester. If more resistance is needed, the data signal to control circuit **28** may be set to logic zero. The control signal to transistor **30** goes low as described above for control circuit **24**. Transistor **30** turns off and enables the conduction through resistor **16**. The resistance of ladder **10** increases to $R_{MIN}+R_{14}+R_{16}$, where R_{16} is the value of resistor **16**. Again, the effect of the added resistance on the operation of the circuit under test may be checked and verified by the tester. The process continues until the circuit under test operates as desired. Note at this point, the trimming process is temporary and dependent on the data signals to control circuits **24**, **28** and **32**. No fuses have yet been blown to lock in the trim. Thus, different combinations of resistors **14**–**18** may be previewed and checked to achieve optimal results.

An alternate trim approach could initially set the data signals to logic zero in control circuits **24**, **28** and **32**. The output of each OR gate **42** goes low and disables transistors **26**, **30** and **34**. The shunt elements **26**, **30** and **34** are substantially opened, i.e. enabling conduction through resistors **14**–**18**, thereby making ladder **10** resistance maximum. The testing preview involves setting the data signals to logic one and iteratively enabling transistors **26**, **30** and **34** to disable conduction through resistors **14**–**18** and reduce resistance in ladder **10**. The process continues until the circuit under test operates as desired. Again, the trimming process is temporary and dependent on the data signals to control circuits **24**, **28** and **32**. No fuses have yet been blown to lock in the trim. Different combinations of resistors **14**–**18** may be tried and checked to achieve optimal results.

Another embodiment of the present invention is to configure the resistor ladder with the resistors in parallel and the control transistors in series with each resistor.

For the circuits under test that functionally pass, the bit pattern of trim is recorded in a file by wafer and die site. The file accompanies the wafer to a laser fuse system where the selected fuses **46** are blown. Once the appropriate fuses are blown, the latches in the control circuits are set to logic zero so that the state of the fuses alone determines the state of the control signal and therefore the permanent trim. The control signals from control circuits **24**, **28** and **32** are thus set to a fixed value by blowing the selected fuses **46** in the control circuits after removal of the data signal at terminal **22**.

The fuses are generally doped polycrystalline silicon films sometimes silicided polycrystalline silicon films in the range of 10 to 500 ohms. The polysilicon film is usually made in the shape of a polysilicon resistor with a width five to ten times its length. The ends of the fuses are connected by metal interconnects to the relevant circuitry. The fuse usually has most or all overlying oxide layers removed. With the use of on-die alignment marks the laser beam of approximately 1 μm–2 μm beam width is focused on the center of the fuse. The laser beam is a pulsed signal of such an energy that the polysilicon is vaporized and the fuse is severed and therefore permanently no longer conductive.

A key feature of the present invention is to preview trimming at wafer test to provide an economical means of iteratively trimming the resistive ladder using data provided by the tester. A data signal selectively trims the resistor ladder. The trimming is temporary and may be modified with different data signals to achieve optimal results. When the proper pattern of trim bits is determined for each individual circuit under test, that data is recorded and transferred off-line to the laser trimmer along with the wafer. The laser trim system blows the appropriate fuses for each circuit under test according to the pattern previously determined by testing various trimming options. Once the appropriate fuses are blown, the latches in the control circuits are set to logic zero so that the state of the fuses alone determines the state of the control signal and therefore sets the permanent trim. The preview trimming process allows optimization of the bit pattern for trimming before the actual laser trimming. Furthermore, the testing and the fusing systems may remain separate without requiring multiple passes through each.

While specific embodiments of the present invention have been shown and described, further modifications and improvements will occur to those skilled in the art. It is understood that the invention is not limited to the particular forms shown and it is intended for the appended claims to cover all modifications which do not depart from the spirit and scope of this invention.

I claim:

1. An analog trim circuit, comprising:

a passive element having first and second conduction terminals;

first means coupled across said passive element and operating in response to a control signal for enabling and disabling conduction through said passive element, said first means includes a transistor having a gate, a drain and a source, said drain being coupled to said first conduction terminal, said

source being coupled to said second conduction terminal, said gate being coupled for receiving said control signal; and

second means responsive to a data signal for providing said control signal to said first means to enable and disable said conduction through said passive element, said second means setting said control signal to a fixed value after removal of said data signal.

2. The analog trim circuit of claim 1 wherein said passive element includes a first resistor coupled between said first and second conduction terminals.

3. The analog trim circuit of claim 2 wherein said second means includes:

a latching circuit having an input coupled for receiving said data signal and having an output;

a logic gate having first and second inputs and an output, said first input being coupled to said output of said latching circuit, said output being coupled for providing said control signal;

a second resistor coupled between a first power supply conductor and said second input of said logic gate; and

a fuse coupled between said second input of said logic gate and a second power supply conductor.

4. A method of analog trimming, comprising the steps of:

enabling conduction through a passive element in response to a first state of a control signal;

disabling conduction through said passive element in response to a second state of said control signal;

activating said control signal in response to a data signal to enable and disable said conduction through said passive element, said activating step including the steps

(a) latching said data signal, and

(b) logically combining said data signal with a logic signal for providing said control signal; and

setting said control signal to a fixed value after removal of said data signal.

5. The method of claim 4 wherein said setting step includes the steps of:

removing said data signal; and

blowing a fuse to set said control signal at said fixed value.

6. An analog trim circuit, comprising:

a passive element having first and second conduction terminals;

a transistor having a gate, a drain and a source, said drain being coupled to said first conduction terminal, said source being coupled to said second conduction terminal, said gate being coupled for receiving a control signal;

a latching circuit having an input coupled for receiving a data signal and having an output;

a logic gate having first and second inputs and an output, said first input being coupled to said output of said latching circuit, said output being coupled for providing said control signal;

a first resistor coupled between a first power supply conductor and said second input of said logic gate; and

a fuse coupled between said second input of said logic gate and a second power supply conductor.

7. The analog trim circuit of claim 6 wherein said passive element includes a first resistor coupled between said first and second conduction terminals.

* * * * *

Exhibit D

United States Patent [19]

Schuster et al.

[11] Patent Number: 5,000,827

[45] Date of Patent: Mar. 19, 1991

[54] METHOD AND APPARATUS FOR ADJUSTING PLATING SOLUTION FLOW CHARACTERISTICS AT SUBSTRATE CATHODE PERIPHERY TO MINIMIZE EDGE EFFECT

[75] Inventors: Virgil E. Schuster; Reginald K. Asher, Sr., both of Scottsdale; Bhagubhai D. Patel, Tempe, all of Ariz.

[73] Assignee: Motorola, Inc., Schaumburg, Ill.

[21] Appl. No.: 459,892

[22] Filed: Jan. 2, 1990

[51] Int. Cl.[5] C25D 5/02

[52] U.S. Cl. 204/15

[58] Field of Search 204/15

[56] References Cited

U.S. PATENT DOCUMENTS

4,287,029 9/1981 Shimamura 204/15

FOREIGN PATENT DOCUMENTS

28039 3/1978 Japan .
123089 5/1989 Japan .
198017 8/1989 Japan .
242797 9/1989 Japan .

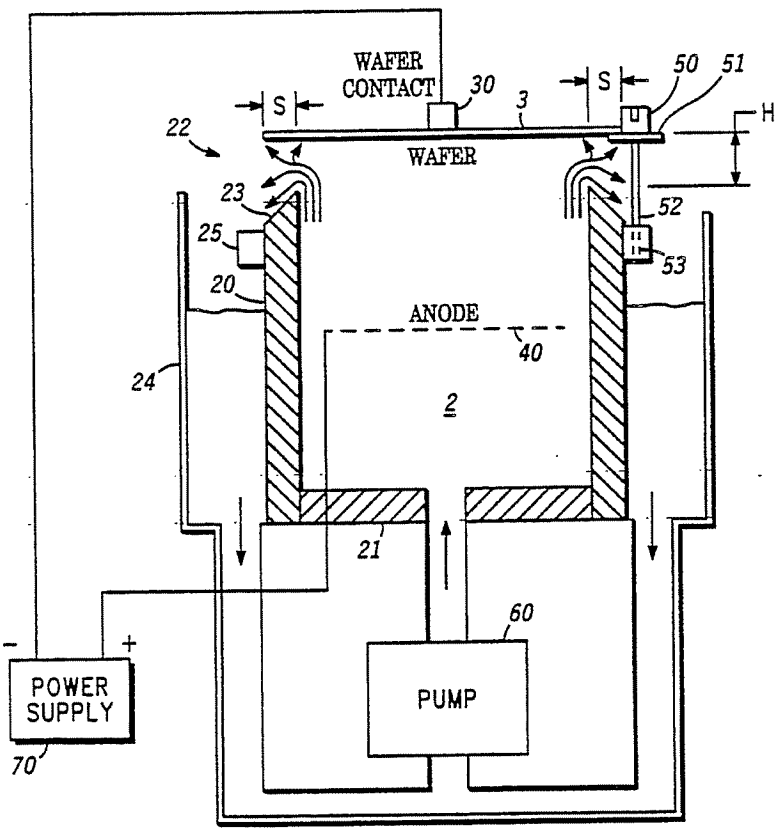
Primary Examiner—T. M. Tufariello

Attorney, Agent, or Firm—Charles R. Lewis; Walter W. Nielsen

[57] ABSTRACT

A method and apparatus for electroplating metallized bumps of substantially uniform height on predetermined terminal areas of a substrate. Cup plating apparatus includes elements for adjusting parameters affecting the geometry of the substrate relative to the plating cup, as well as flow rate of the electroplating solution against the substrate surface. By achieving non-laminar flow of the electroplating solution near the substrate edges, the plating characteristics of the electroplating solution are altered in this region, substantialy offsetting "edge effect", so that the resulting plated bump height is substantially uniform across the substrate.

2 Claims, 7 Drawing Sheets



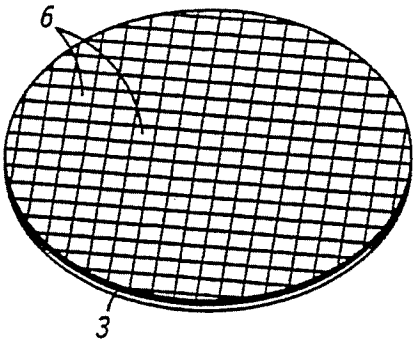


FIG. 1

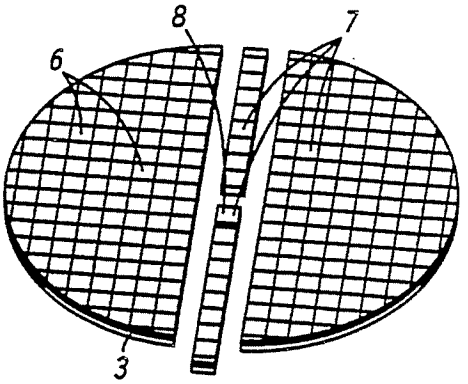


FIG. 2

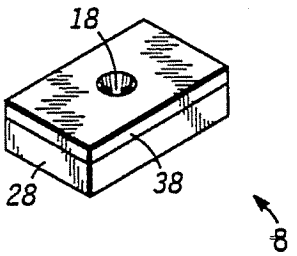


FIG. 3A

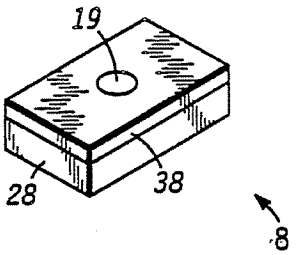


FIG. 3B

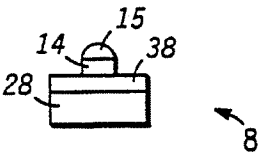


FIG. 3C

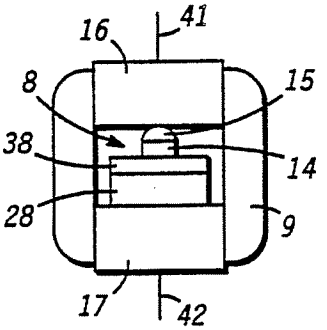


FIG. 4

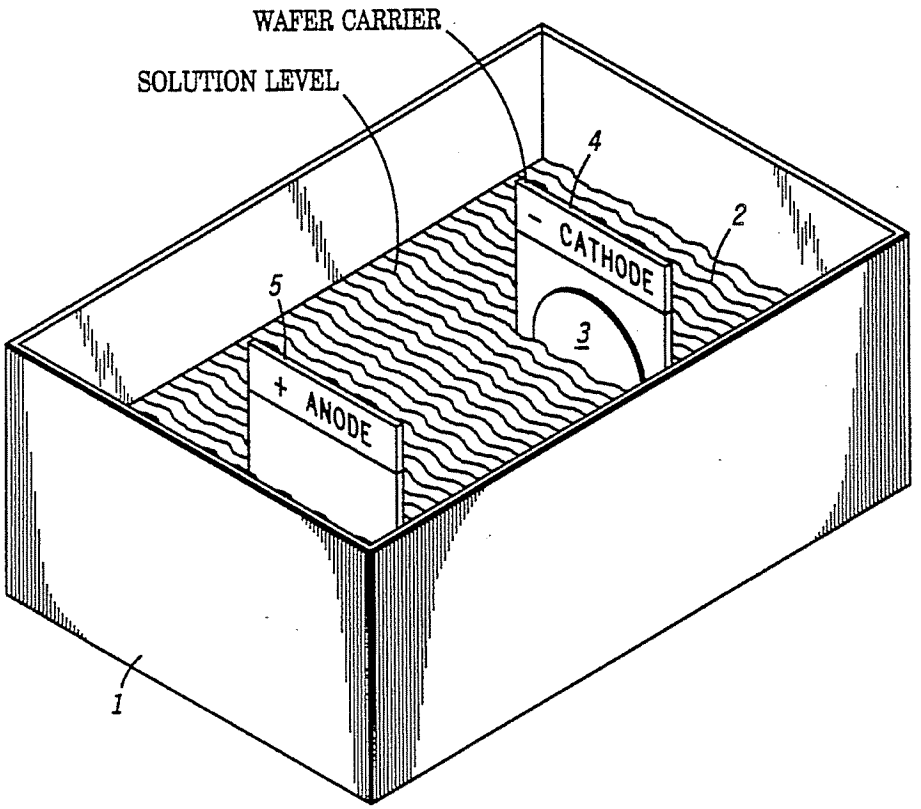
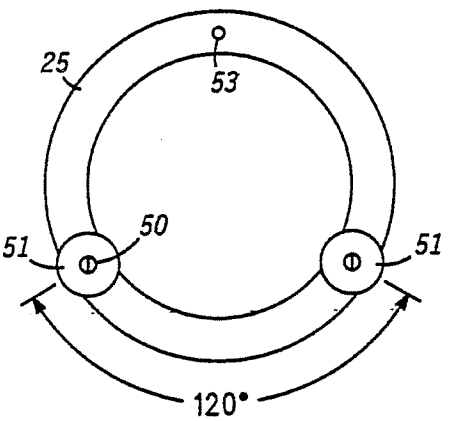
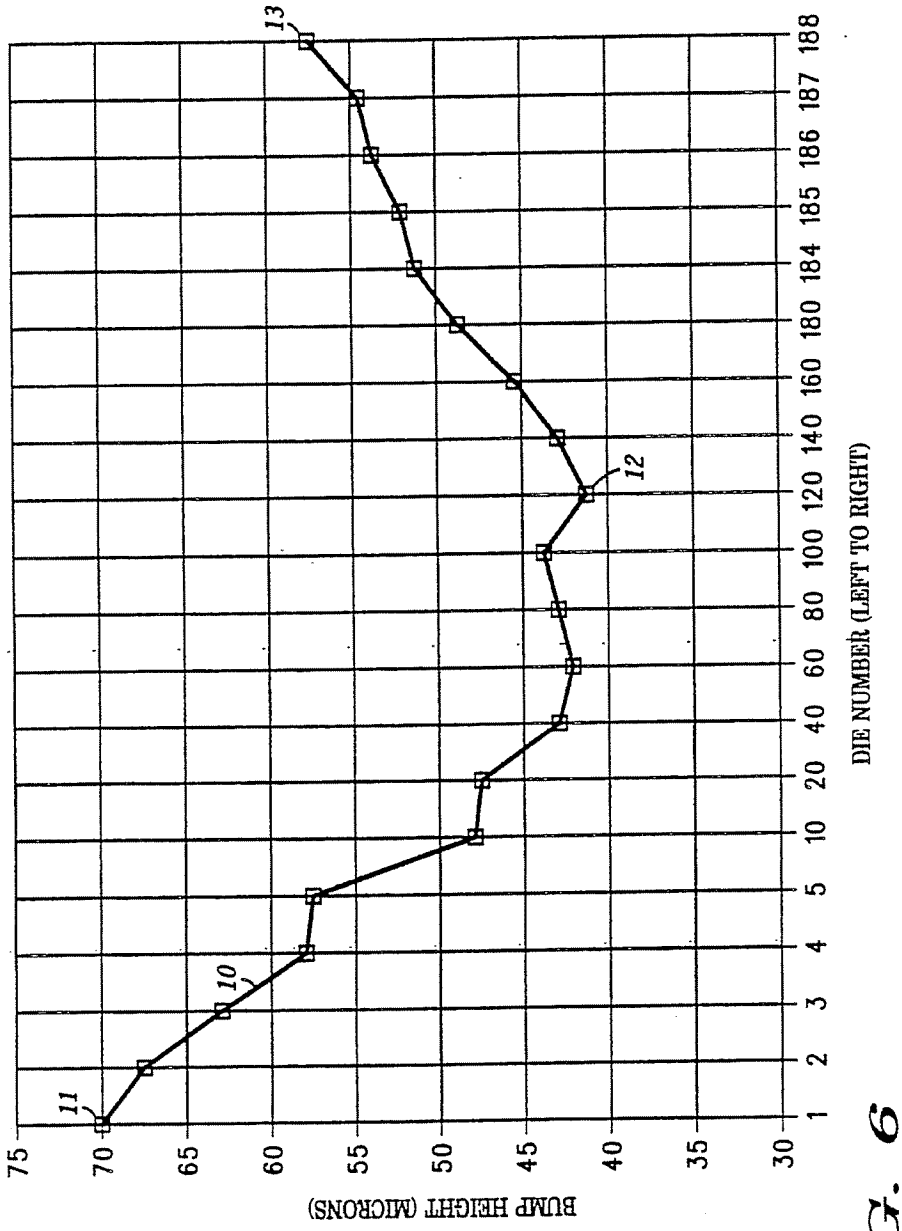


FIG. 5
-PRIOR ART-

FIG. 8

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184
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186
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188
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11
12
13

FIG. 6

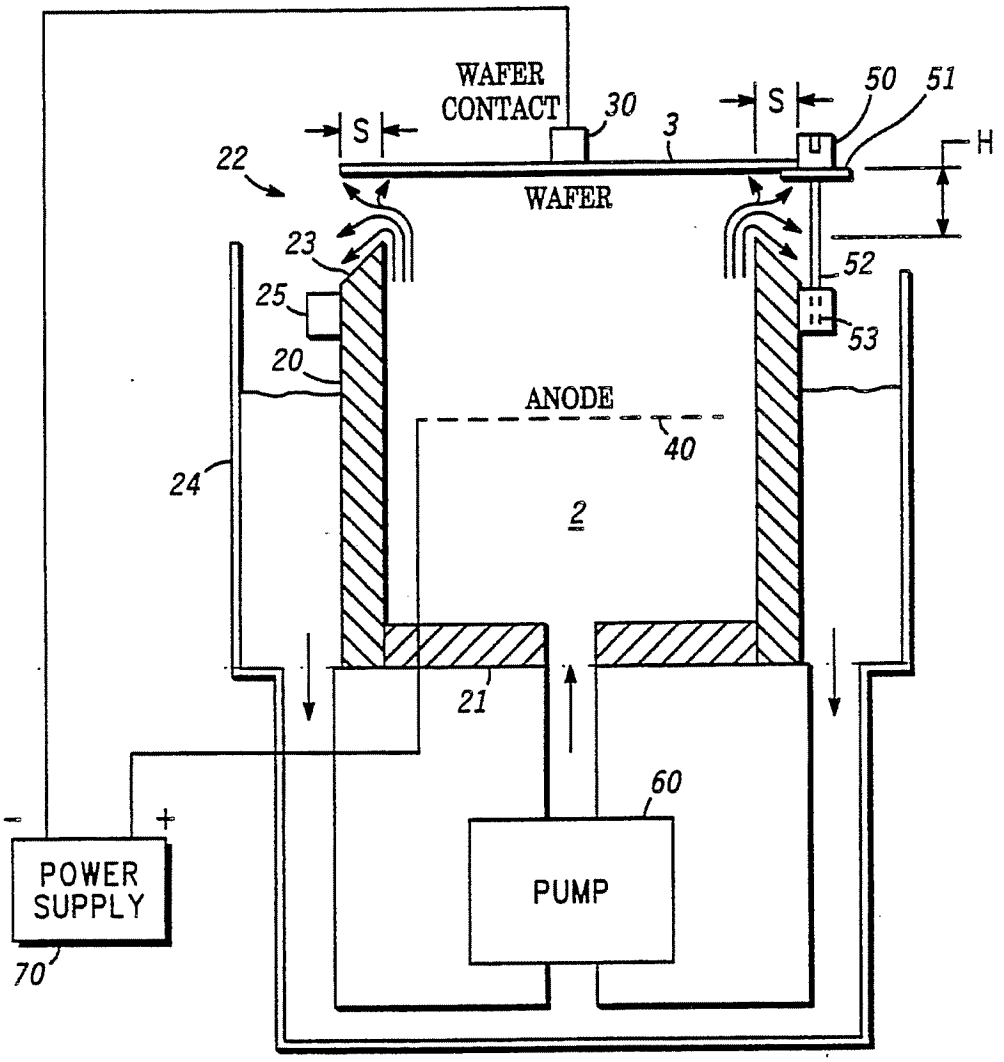
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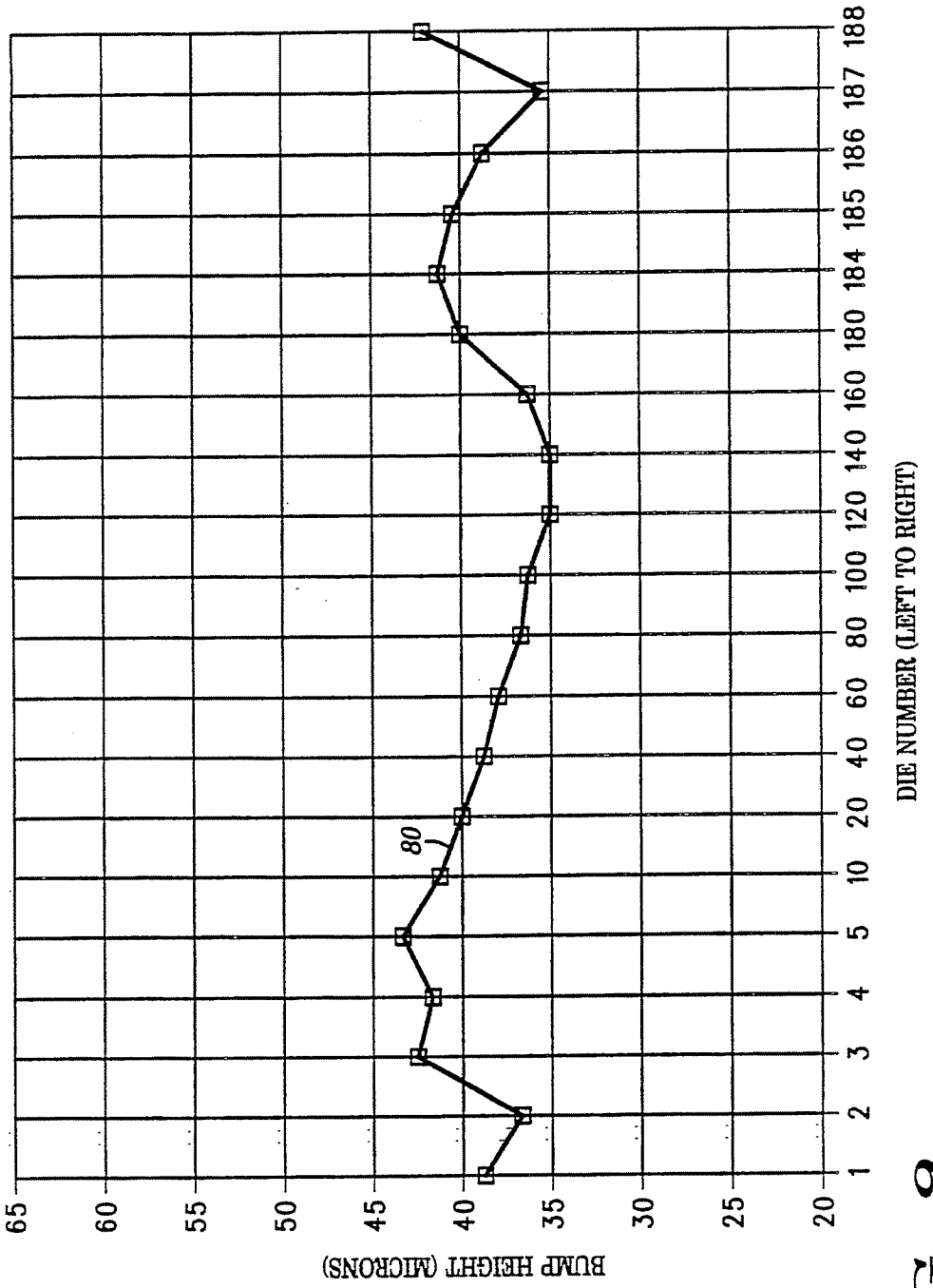
FIG. 7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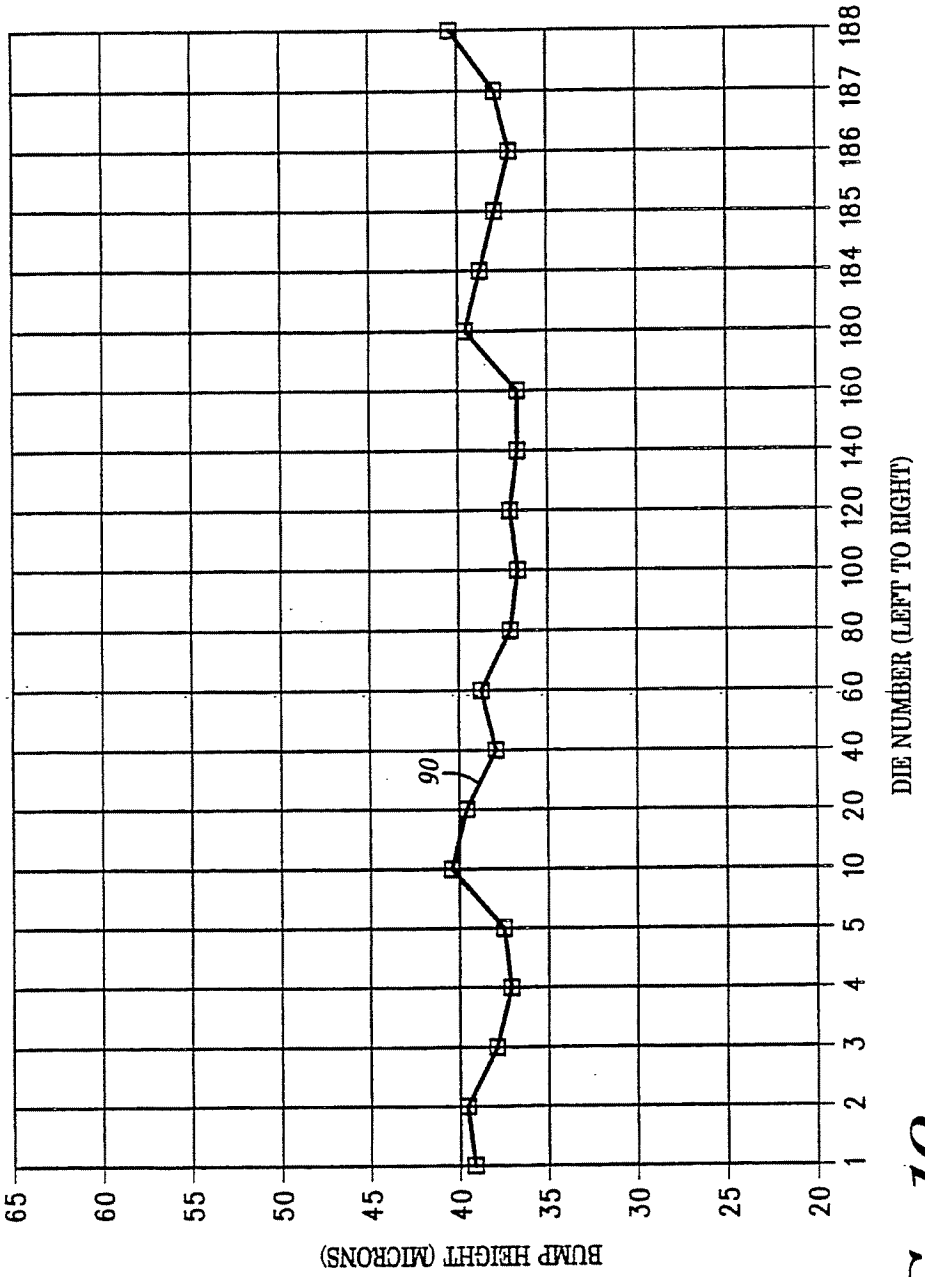
DIE NUMBER (LEFT TO RIGHT)

FIG. 9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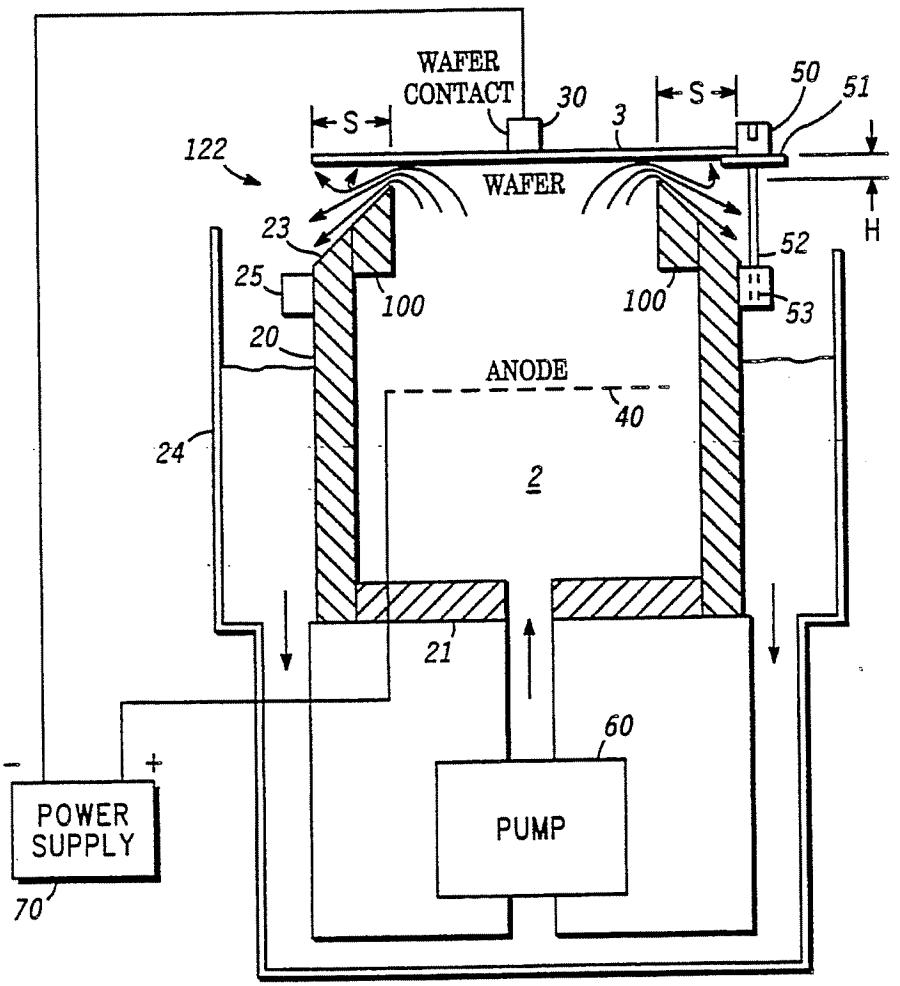
186
187
188
DIE NUMBER (LEFT TO RIGHT)
90

FIG. 10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PUMP
70

FIG. 11

METHOD AND APPARATUS FOR ADJUSTING PLATING SOLUTION FLOW CHARACTERISTICS AT SUBSTRATE CATHODE PERIPHERY TO MINIMIZE EDGE EFFECT

BACKGROUND OF THE INVENTION

1. Technical Field of the Invention

This invention relates generally to the manufacture of micro-electrical circuits, and, more particularly, to the formation of uniform-thickness metallization bumps on terminal areas of electrical circuits on a substantially planar substrate, particularly near the edge thereof.

2. Background Information

The present invention has utility in the plating of metallization bumps on predetermined terminal areas of silicon wafers prior to scribing such wafers into a plurality of individual die.

FIG. **1** shows a silicon wafer **3** upon which a plurality of individual electrical circuit elements **6** are formed. The electrical characteristics of individual circuit elements **6** may be imparted to them by employing any suitable process(es) therefor. The specifics of the electrical circuit of the circuit elements **6** lies outside of the scope of the present invention.

FIG. **2** shows a view similar to that shown in FIG. **1**, wherein the wafer **3** has been separated into pieces **7** including at least one die **8** using conventional wafer scribing or sawing techniques.

FIGS. **3**A show steps in the formation of a terminal region **19** on a surface of an individual die **8**, prior to wafer scribing or sawing, and the plating of a metallization bump onto such terminal region **19**. In the manufacture of a particular electrical product from die **8**, such as the double-slug diode shown in FIG. **4**, it is frequently necessary to deposit a metallized bump in a predetermined area of a surface of such die.

Referring to FIG. **3**A, a representative individual die **8** of wafer **3** is shown overlaid with a layer of oxide **38**, and a hole or window **18** has been etched through the oxide **38** down to a terminal area (not shown) of the underlying substrate **28**.

In FIG. **3**B, the window **18** of FIG. **3**A has been filled with top metal **19**. In a preferred embodiment of the invention, the top metal **19** actually comprises three layers: first a layer of titanium, next a layer of nickel, and finally a layer of silver. Again, the composition of the layers and thickness thereof are not specific to the present invention.

In FIG. **3**C, a metallization bump, comprising a layer of silver **14** and a layer of tin **15**, has been electro-deposited over the top metal terminal region **19**.

FIG. **4** shows a double-slug diode manufactured according to the method and apparatus disclosed by the present invention. The diode of FIG. **4** is shown for illustrative purposes only, and it should be understood by all practitioners in the art that the present invention has broad utility in many metallization bump processing applications and is not intended to be limited to implementations such as that shown in FIGS. **3** and **4**.

Still with reference to FIG. **4**, the die **8** has been separated from its counterparts on wafer **3** and mounted between copper "slugs" or terminals **16** and **17** to which electrical leads **41** and **42**, respectively, have been affixed. The entire assembly is enclosed in glass **9**.

FIG. **5** shows a prior art plating apparatus for plating metallization bumps onto predetermined terminal areas of a silicon wafer, such as terminal area **19** of die **8**.

Referred to as a rack plating apparatus, it comprises a tank **1** of electroplating solution into which an anode **5** and a cathode **4** are shown partially submersed. It will be understood that anode **5** and cathode **4** are shown partially submersed for ease in understanding and that during operation they are substantially submersed.

Anode **5** has a potential having a positive polarity coupled thereto, while cathode **4** has a potential having a negative polarity coupled thereto.

Affixed to cathode **4** is a substantially planar, conductive wafer **3** comprising a plurality of individual electrical elements (not shown), each with a terminal area such as terminal area **19** shown in FIG. **3**B. It will be understood by those skilled in the art that substrate **3** may itself serve as the cathode **4**, or substrate **3** may be suitably affixed to a wafer carrier, which serves as the cathode **4**.

FIG. **6** is a graph illustrating the variation of bump height across a silicon wafer electroplated with the prior art plating apparatus shown in FIG. **5**. The bump height in microns measured on selected die is provided along the Y-axis, and the die position across a given wafer diameter is provided along the X-axis. It will be observed that the X-axis of FIG. **6** is non-linerar, in that emphasis is given to die numbers closest to the wafer edge, for example die numbers **1–5** at the left edge and die number **184–188** at the right edge.

It is seen that when metallized bumps are plated with the apparatus shown in FIG. **6** there is substantial variation in bump height across the wafer diameter. The bumps are highest at or near the wafer edge. For example, the bump height **11** of die #**1** is 70 microns, and that of die #**188** is approximately 58 microns, whereas that of die #**120** is approximately 41 microns.

According to the graph of FIG. **6**, the bump height variation across a typical 9.65 centimeter diameter wafer is almost 30 microns, ranging from a minimum of 41 microns at die #**120** to a maximum of 70 microns at die #**1**. This greatly exceeds a desired production specification width of 20 microns.

The increased electroplating intensity near the wafer edge is commonly referred to as "edge effect".

Therefore, there is a substantial need to provide an electroplating method and apparatus which overcomes the "edge effect" problem known in prior electroplating systems.

Various electroplating systems are known which have attempted to overcome the "edge effect". One such system is referred to as a cathode-mask system, in which the high-growth area of the substrate is masked. However, this system suffers from the need to achieve critcal positioning of the mask relative to the high-growth area of the substrate. Both the alignment of the mask and the mask-to-wafer spacing are critical and difficult to control.

BRIEF SUMMARY OF INVENTION

The present invention solves the problem of "edge effect" by selectively altering the metallic ion concentration of the electroplating solution near the edge(s) of the wafer substrate.

According to the present invention, the electroplating solution is contained in a cup-shaped container. A pump circulates the solution through an inlet and out over the lip of the cup. The wafer is suspended at an optimum height above the cup lip. The cup diameter is optimized relative to the wafer diameter and to the area

in which undue bump growth occurs. In addition, the flow rate of solution through the plating cup is optimized. By optimizing the above-mentioned parameters, the metallic ion concentration of the electroplating solution in the vicinity of the wafer edge(s) is optimized to just offset the "edge effect", and to provide substantially uniform height of electroplated bumps across the wafer diameter.

Accordingly, it is an object of the present invention to provide an electroplating method and apparatus which produce metallized bumps of substantially uniform height across a substrate including the edge(s) thereof.

Thus a greater proportion of die fall within desired specifications, resulting in lower rejection rates, lower material and labor charges, higher quality, and greater customer acceptance.

It is another object of the present invention to provide an electroplating method and apparatus which is relatively inexpensive and which is relatively easy to control.

It is yet another object of the present invention to provide an electroplating method and apparatus which eliminates the labor-intensive steps of mounting a substrate on a wafer carrier prior to electrodepositing the metallized bumps, demounting the substrate from the wafer carrier after deposition, and cleaning the mounting agent (typically wax, glycol, or plastic) from the substrate.

These and other objects are achieved in accordance with a preferred embodiment of the invention by providing a method of forming metallization bumps on predetermined terminal areas of a planar substrate, the bumps being of substantially uniform height across the substrate, wherein the method comprises (a) providing a planar substrate having thereon a multiplicity of terminal areas; (b) applying an electrical potential having a first electrical polarity to the terminal areas; (c) applying an electrical potential having a second electrical polarity to an electrical terminal immersed in a container of an electroplating solution; (d) exposing the substrate to the electroplating solution to permit the growth of the metallization bumps on the terminal areas: and (e) controlling the growth of the metallization bumps in a predetermined region of the substrate by altering the metallic ion concentration of the electroplating solution in the predetermined region.

BRIEF DESCRIPTION OF THE DRAWINGS

The invention is pointed out with particularity in the appended claims. However, other features of the invention will become more apparent and the invention will be best understood by referring to the following detailed description in conjunction with the accompanying drawings in which:

FIG. 1 shows a silicon wafer upon which a plurality of individual electrical circuit elements are formed.

FIG. 2 shows a view similar to that shown in FIG. 1, wherein the wafer has been separated into pieces including at least one die.

FIGS. 3A, 3B and 3C show steps in the plating of a metallization bump onto a terminal area of an individual die.

FIG. 4 shows a double-slug diode manufactured according to the method and apparatus disclosed by the present invention.

FIG. 5 shows a prior art plating apparatus for plating metallization bumps onto predetermined terminal areas of a silicon wafer.

FIG. 6 is a graph illustrating the variation of bump height across a silicon wafer electroplated with the prior art plating apparatus shown in FIG. 5.

FIG. 7 shows a cross-sectional view of apparatus for plating metallization bumps of substantially uniform height onto predetermined terminal areas of a silicon wafer, according to the present invention.

FIG. 8 shows a top-view of ring element 25 and adjustable wafer support elements 51 of the plating apparatus shown in FIG. 7.

FIG. 9 is a graph illustrating the variation of bump height across a silicon wafer electroplated according to the method of the present invention.

FIG. 10 is another graph illustrating the variation of bump height across a silicon wafer electroplated according to the method of the present invention.

FIG. 11 shows a cross-sectional view of an alternative embodiment of apparatus for plating metallizaton bumps of substantially uniform height onto predetermined terminal areas of a silicon wafer, according to the present invention.

DESCRIPTION OF PREFERRRED EMBODIMENT

FIG. 7 shows apparatus for plating metallization bumps of substantially uniform height onto predetermined terminal areas of a silicon wafer, according to the present invention. A cylcindrical cup 20 of suitable material, such as polyvinylchloride (PVC) or polypropylene, contains the desired electroplating solution, which in a preferred embodiment is a cyanide silver plating solution. The bottom portion of cup 20 may be formed integrally therewith or may be formed separately, as shown by bottom portion 21.

Pump 60 circulates the plating solution 2 through an inlet in the bottom cup 20, and plating solution 2 exists cup 20 over the lip 23 into tank or sump 24, from which it is eventually returned to the inlet side of pump 60.

To a suitable power supply 70, such as a pulsing DC rectifier, are coupled a wafer contact 30 and an anode 40. Anode 40 may take the form of a platinum-clad tantalum screen immersed in the electroplating solution. Wafer contact 30 may take the form of a silver-clad nickel element which rests upon or is affixed to the upper surface of water or substrate 3. Wafer 3 functions as a cathode.

Wafer 3 is supported by several wafer support members 51 suitably mounted in a ring or collar member 25 around the periphery of cup 20 (refer to FIG. 8). Support member 25 may take the form of a PVC washer mounted on a PVC screw 52, having a slotted head 50, and being threaded into a mating opening 53 in ring 25.

FIG. 8 shows a top-view of ring element 25 and adjustable wafer support elements 51 of the plating apparatus shown in FIG. 7. In a preferred embodiment, three wafer support elements 51 are spaced substantially equidistantly around the periphery of ring 25, and each has a slotted head to facilitate adjusting the height of wafer 3 above the lip 23 of cup 20.

Operation of Preferred Embodiment

In operation, as mentioned above, electroplating solution 2 flows generally upwards from the inlet in the bottom of cup 20, against the underside of wafer 3, and out over the lip 23 into sump 24.

Cup plating apparatus is known in the art and, as used, suffers from the well-known "edge effect". However, according to the present invention the metallic ion concentration of electroplating solution 2 is altered in the region near the edge of wafer 3, so as to effectively offset the "edge effect".

By creating non-laminar flow of the electroplating solution 2 through the opening between the lip 23 and lower surface of wafer 3, the plating characteristics of solution 2 near the edge are altered from those elsewhere within cup 20. The plating effect of the solution is weakened, thereby offsetting the tendency for increased plating effect near the cathode edge. The precise reasons as to why turbulent flow of the electroplating solution 2 against the outer portions of wafer 3 causes an offsetting of the "edge effect" are not completely understood.

To produce the non-laminar flow over the optimum peripheral area of wafer 3, the distance S between the outer edge of wafer 3 and the inner surface of cup 20 should be optimized. The parameter S is changed by changing the diameter of cup 20 relative to the diameter of wafer 3. By decreasing the diameter, a relatively greater peripheral area of wafer 3 is affected by a slight reduction in bump growth rate, whereas increasing the diameter of cup 20 diminishes the peripheral area of wafer 3 which is affected. In a preferred embodiment of the invention, the diameter of the wafer was 9.65 centimeters, and the inside diameter of the cup was 8.89 centimeters.

Another important dimension which should be optimized is the distance H between the lower surface of wafer 3 and the top of cup lip 23. If H is too low, laminar flow apparently results, and there is relatively little offsetting of the "edge effect", resulting in relatively higher bumps near the edge. As H is increased, turbulent flow apparently results, perhaps due to the capillary attraction of the bottom surface of wafer 3 near the edge, and there is increased offsetting of the "edge effect", resulting in edge bumps which are nearly identical in height to bumps elsewhere across the wafer diameter (refer to FIG. 10).

Flow rate through the plating cup 20 was found not to be a critical parameter. In a preferred embodiment, a flow rate of 4 to 5 liters/minute was employed.

The invention described herein was used successfully to plate bumps comprising an initial layer of silver and a subsequent layer of tin, resulting in metallization bumps substantially as depicted in FIG. 3C.

FIG. 9 is a graph illustrating the variation of bump height across a silicon wafer electroplated according to the method of the present invention. To produce the results illustrated in FIG. 9, the height H of wafer 3 above the lip 23 of cup 20 was set at 2.25 millimeters. This produced a bump height variation across the wafer ranging from a high of 43 microns to a low of 35 microns (i.e. with a process variation of approximately 8 microns), which is well within a desired specification width of 20 microns.

FIG. 10 is another graph illustrating the variation of bump height across a silicon wafer electroplated according to the method of the present invention. By raising the height H of wafer 3 above the lip 23 of cup 20 to 2.45 millimeters, the bump height variation across the wafer ranged from a high of 40 microns to a low of 36 microns (i.e. with a process variation of approximately 4 microns). This is a substantial improvement over the process variation of 30 microns produced by the known tank electroplating method.

Description of Alternative Embodiment

FIG. 11 shows an alternative embodiment of apparatus for plating metallization bumps of substantially uniform height onto predetermined terminal areas of a silicon wafer, according to the present invention.

The apparatus illustrated in FIG. 11 differs from that shown in FIG. 7 only in that the distance S between the outer edge of wafer 3 and the inner surface of cup 20 has been increased through the use of an annular ring 100 suitably secured within the lip portion 23 of cup 20. This is shown merely as one example of how the distance S may be altered.

It will be apparent to those skilled in the art that the disclosed invention may be modified in numerous ways and may assume many embodiments other than the preferred form specifically set out and described above.

For example, the present invention can be extended to electroplating of ceramic substrates. It may also be extended to electroplating metals other than those mentioned herein. The plating cup may take the form of a pipe or other suitable geometric shape.

Accordingly, it is intended by the appended claims to cover all modifications of the invention which fall within the true spirit and scope of the invention.

What is claimed is:

1. A method of forming metallized bumps on predetermined terminal areas of a planar substrate, said bumps being of substantially uniform height across said substrate, wherein said method comprises:

(a) providing a planar substrate having thereon a multiplicity of terminal areas;

(b) applying an electrical potential having a first electrical polarity to said terminal areas;

(c) applying an electrical potential having a second electrical polarity to an electrical terminal immersed in a container of an electroplating solution;

(d) exposing said substrate to said electroplating solution to permit the growth of said metallization bumps on said terminal areas;

(e) controlling the growth of said metallization bumps in a predetermined region of said substrate by altering the metallic ion concentration of said electroplating solution in said predetermined region;

(f) providing said container with an opening whose shape approximates that of said substrate;

(g) positioning said substrate proximate to said container opening;

(h) providing an inlet within said container for pumping said solution into said container, said solution exiting said container through said opening;

wherein said metallic ion concentration of said electroplating solution is changed by:

(i) in step (f) altering the size of said opening;

(j) in step (g) altering the distance of said substrate from said container opening; and

(k) in step (h) altering the flow rate of said solution through said opening.

2. The method of according to claim 1, wherein said metallization bumps comprise metal selected from the group consisting of silver and tin.

* * * * *

EXHIBIT-E

US005252177A

United States Patent [19]

Hong et al.

[11] Patent Number: 5,252,177

[45] Date of Patent: Oct. 12, 1993

[54] METHOD FOR FORMING A MULTILAYER WIRING OF A SEMICONDUCTOR DEVICE

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[21] Appl. No.: 736,772

[22] Filed: Jul. 29, 1991

[30] Foreign Application Priority Data

Apr. 15, 1991 [KR] Rep. of Korea 1991-6024

[51] Int. Cl.[5] B44C 1/22; C23F 7/00

[52] U.S. Cl. 156/643; 156/644; 156/657; 156/656; 156/667; 204/192.32; 437/228; 437/235

[58] Field of Search 156/643, 644, 651, 652, 156/655, 656, 657, 659.1, 662, 667; 204/192.32, 192.35; 437/180, 187, 198, 199, 203, 228, 235, 238

[56] References Cited

U.S. PATENT DOCUMENTS

4,857,141 8/1989 Abe et al. 156/644

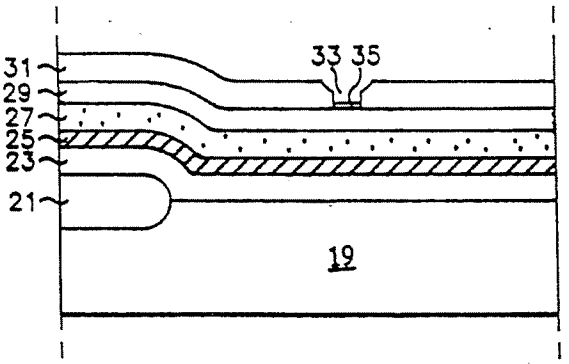
Primary Examiner—William A. Powell

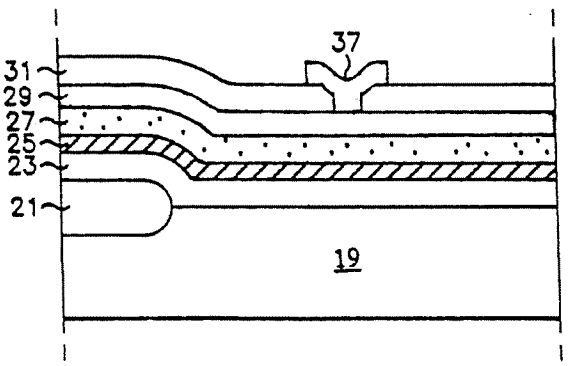
Attorney, Agent, or Firm—Robert E. Bushnell

[57] ABSTRACT

A method for forming a multilayer wiring, in a method for manufacturing a semiconductor device, is disclosed. The method comprises: forming a contact hole **33** on the surface of a conductive layer **29** by a photolithography, removing a photoresist by using plasma ashing at a predetermined temperature, pressure and amount of oxygen per unit cubic, and simultaneously forming a protective layer **35** consisting of a oxide layer on the surface of the exposed conductive layer. Thus, damage of the surface of wiring caused by the chemical reaction of an organic solvent and water in the subsequent process thereof, is prevented, to provide high density and high speed semiconductor integrated circuit whose electrode characteristics between two wiring layers is improved.

15 Claims, 2 Drawing Sheets





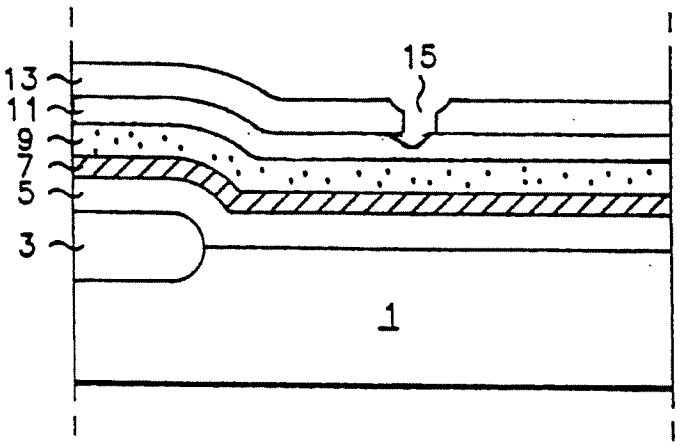


Fig. 1A
(Prior Art)

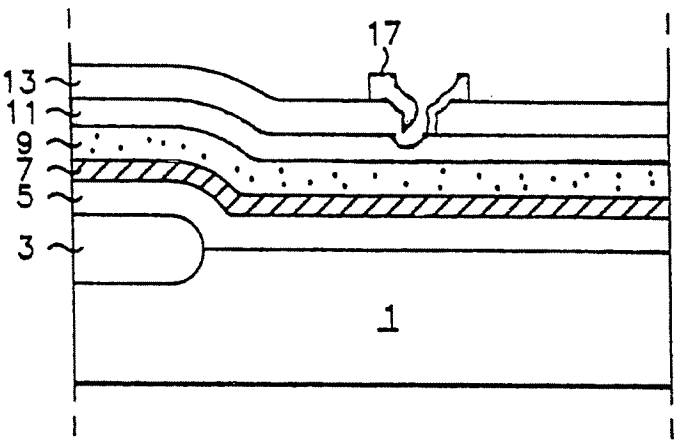


Fig.1B
(Prior Art)

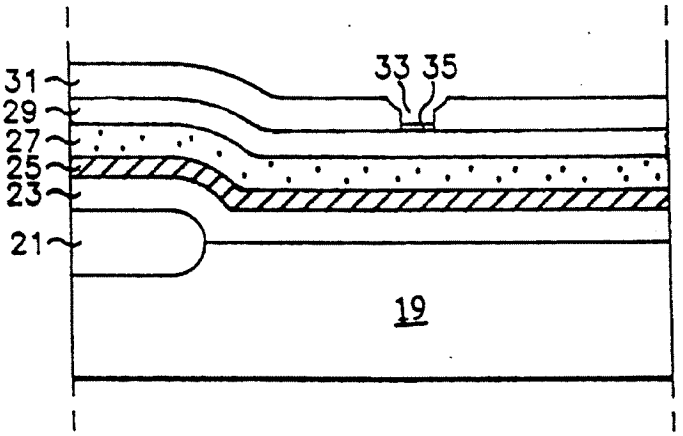


FIG. 2A

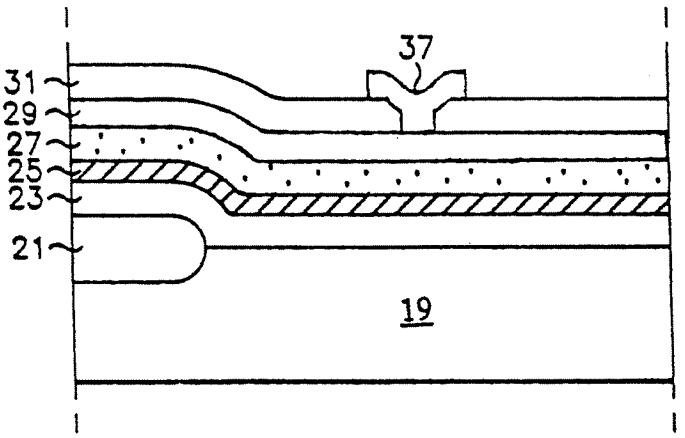


FIG. 2B

METHOD FOR FORMING A MULTILAYER WIRING OF A SEMICONDUCTOR DEVICE

FIELD OF THE INVENTION

The present invention relates to a method for manufacturing a semiconductor device, and more particularly to a method for forming multilayer wiring.

BACKGROUND OF THE INVENTION

Recently, the density of semiconductor devices and operating speeds thereof have been increased. However, in case of a semiconductor integrated circuit having conventional one layer wiring, a reduction in the width of metal wiring in the memory device increased electrical resistance. Thus, the power consumption increases. Accordingly, to enhance operating speed, multilayer wiring has been proposed. A material metal wiring is aluminum containing silicon of under 4% to prevent aluminum spike occurred when forming wiring with pure aluminum. However, aluminum wiring containing added copper added has been proposed to improve reliability.

FIGS. 1A and 1B illustrate a conventional method for manufacturing a semiconductor device having multilayer wiring. In the FIG. 1A, on a semiconductor substrate 1 of a first conductivity type, where field oxide layer 3 for isolation is formed, a first insulation layer 5, a first conductive layer 7, a second insulation layer 9, a second conductive layer **11** and a third insulation layer 13 are consecutively deposited. Then, a contact hole 15 is formed through selective etching of the third insulation layer 13 by photolithography. Thus, the top surface of the second conductive layer 11 is partially exposed. Here, the first conductive layer 7 is bit line, and the second conductive layer 11 is aluminum wiring containing silicon of about 1% and copper of about 0.5%. By employing the above mentioned aluminum in the metal wiring, hillock and electromigration characteristics can be improved as compared with conventional aluminum wiring containing only silicon. The wiring made of the second conductive layer 11 and another wiring (not shown) are contacted through the contact hole 15. In forming the described wiring of multilayer structure, in practice, underlying layer wiring can be damaged by the chemical reaction of copper component extracted into the grain boundary of the aluminum, water (H_2O) and organic solvents, etc, which occur during removal of the ordinary photoresist. That is, to expose the surface of the underlying layer wiring, plasma ashing (process of developing a photoresist and thereafter removing the photoresist remaining after plasma etching process), dipping in an organic solvent such that sulfate acid, rinsing with water and drying are progressively carried out to remove the remaining photoresist positioned on the upper surface of the insulation layer. At this time, the exposed portions of aluminum wiring containing copper directly contact the organic solvent and water. As a result, the copper component existing in grain boundary of the aluminum is discolored with black spots and pieces of the second conductive layer **11** may drop away. The size of these pieces can be 1μm in diameter. The resultant damage of the wiring is shown in the FIG. **1A**. When an overlying layer wiring is formed by the vapor deposition and the underlying layer wiring is damaged, step coverage is inferior. Accordingly the overlying layer wiring is shorted or the contact area is decreased

increasing contact resistance. Thus electrical characteristic of devices deteriorates.

FIG. **1B** illustrates the cross sectional view of the conventional multilayer wiring. On the third conductive layer of aluminum, an overlying layer wiring **17** is disposed by formation of a pattern and selective etching. As shown in FIG. **1B**, a portion of the overlying layer wiring contacting the underlying layer wiring small because of the interior step coverage.

As described above, conventional method has a problem that the wiring is damaged by exposure of the underlying layer wiring through the contact hole, when the remaining photoresist disposed over the underlying layer is removed after forming the contact hole on the underlying layer wiring. Therefore, reliable semiconductor integrated circuit is not obtained.

SUMMARY OF THE INVENTION

It is an object of the invention to provide a method for forming a multilayer wiring, and preventing damage of exposed wiring upon removing of a photoresist residue.

To achieve the above object, the method includes the steps of: forming a contact hole for contacting an underlying layer wiring and an overlying layer wiring, removing the remaining photoresist positioned on an insulation layer, the insulation layer being disposed on the underlying layer wiring, by plasma ashing under condition of the predetermined temperature, pressure and amount of oxygen per unit cubic, and simultaneously forming an oxide layer on the exposed underlying layer wiring through the contact hole; and, removing the oxide layer just before forming of the overlying layer wiring.

BRIEF DESCRIPTION OF THE DRAWINGS

The above objects and other advantages of the present invention will become more apparent by describing in detail the preferred embodiment of the present invention with the reference to the attached drawings, in which:

FIGS. **1A** and **1B** are views illustrating conventional manufacturing process; and

FIGS. **2A** and **2B** are views illustrating manufacturing process according to the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

Referring to FIG. **2A**, on the surface of a semiconductor substrate **19**, with a first conductivity type, having field oxide layer **21** formed thereon, a first insulation layer **23**, a first conductive layer **25**, a second insulation layer **27**, a second conductive layer **29** and a third insulation layer **31** are consecutively deposited. Here, the first conductive layer **25** is the bit line, and the second conductive layer **29** is aluminum wiring containing silicon of about 1% and copper of about 0.5%. The wiring is composed of the second conductive layer, and another wiring are contacted through the contact hole **33**. Then, oxygen plasma ashing is performed to remove a remaining photoresist (not shown) positioned on top surface of the third insulation layer **31**. At this time, the process conditions are 500 SCCM (Standard Cubic Centimeter) of oxygen gas, 4–5 Torr of the pressure and 250° C.–350° C. for the temperature of the substrate. As a result, the photoresist is removed, and simultaneously the exposed wiring surface through the contact hole **33**

is oxidized, thereby forming aluminum oxide layer (Al_2O_3) **35** with the thickness of 30Å–80Å. The aluminum oxide layer **35**, an insulation layer, prevents reaction between the wiring, an organic solvent and water in subsequent processing to remove the photoresist, in other words, the dipping in the organic solvent and rinse, etc., Because of the above result, the wiring is protected and not damaged. After removing all the remaining photoresist on the third insulation layer **31**, to form a low resistance contact between the underlying layer wiring and the overlying layer wiring, the aluminum oxide layer **35** is subjected to an ordinary argon sputtering etching.

As shown in FIG. **2B**, an overlying layer wiring **37** is formed by patterning after depositing a third conductive layer of aluminum alloy containing a get amount of copper. Here, the third conductive layer has better step coverage because the underlying layer wiring is undamaged. Accordingly, the contact area between the underlying layer wiring and the overlying layer wiring is maximized, achieving a low resistance contact.

As described above, in the method for forming the multilayer wiring according to the present invention, a protective layer of oxide layer is simultaneously coated on the top exposed surface of the underlying layer wiring, through the contact hole, with removing of the photoresist by photoresist ashing process. Therefore, the damage of the surface of wiring due to chemical reaction of an organic solvent and water in the subsequent process, is prevented so that the underlying layer wiring having better step coverage can be formed. As a result two wiring layers are interconnected with minimum contact resistance drastically enhancing electrode characteristics between the two wiring layers. Accordingly, high-density and high-speed semiconductor integrated circuit having the improved reliability can be obtained.

While the invention has been particularly shown and described with the reference to the preferred embodiment of the present invention thereof, it will be understood by those skilled in the art that the foregoing and other changes in form and details may be made without departing from the spirit and scope of the present invention.

What is claimed is:

1. A method for forming multilayer wiring in a semiconductor device, said semiconductor device comprising a semiconductor substrate and insulation layers and conductive layers formed over a top surface of said semiconductor substrate, said method comprising the steps of:

forming a contact hole by selectively etching out a region of an insulation layer disposed on a first conductive layer using a photoresist pattern to thereby expose a top surface of said first conductive layer;

removing said photoresist pattern positioned on said insulation layer by plasma etching simultaneously forming a protective oxide layer on the exposed top surface of said first conductive layer; and

removing said oxide layer before forming a second conductive layer on said exposed top surface of said first conductive layer.

2. The method as claimed in claim **1**, wherein said first conductive layer is aluminum.

3. The method as claimed in claim **2**, wherein during said plasma ashing, said semiconductor substrate is heated to a temperature of 250°C.–350°C. in a reaction room having an oxygen atmosphere at a pressure of 4-5 Torr.

4. The method as claimed in claim **1**, wherein said oxide layer is aluminum oxide layer and has a thickness of 30Å–80Å.

5. The method as claimed in claim **1**, wherein said oxide layer is removed by argon sputtering etching.

6. The method as claimed in claim **1**, wherein said plasma etching is performed in 500 SCCM of oxygen gas and at a pressure of 4–5 **Torr.**

7. The method as claimed in claim **6**, wherein during said plasma ashing a temperature of said semiconductor substrate is 250°–350° C.

8. A method for forming an electrical connection on a semiconductor substrate between a first conductive layer and a second conductive layer through an intervening insulation layer formed over said first conductive layer, said method comprising the steps of:

forming a photoresist pattern on said insulation layer;

after forming said photoresist pattern, forming a contact hole by selectively etching out exposed regions of said insulation layer to expose a top surface of said first conductive layer;

removing remaining photoresist positioned on said insulation layer by plasma ashing to simultaneously form a protective oxide layer on said exposed top surface of said first conductive layer; and

removing said oxide layer before forming said second conductive layer on said exposed top surface of said first conductive layer.

9. The method as claimed in claim **8**, wherein said plasma ashing is performed in 500 SCCM of oxygen gas and at a pressure of 4–5 Torr.

10. The method as claimed in claim **9**, wherein during said plasma ashing a temperature of said semiconductor substrate is 250°–350° C.

11. The method as claimed in claim **8**, wherein said first conductive layer is mostly aluminum.

12. The method as claimed in claim **8**, wherein said first conductive layer is aluminum containing approximately one percent silicon and approximately one half percent copper.

13. The method as claimed in claim **8**, wherein said protective layer is an aluminum oxide layer.

14. The method as claimed in claim **13**, wherein said protective layer has a thickness of 30Å–80Å.

15. The method as claimed in claim **8**, wherein said protective layer is removed by argon sputtering etching.

* * * * *

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 5,252,177
DATED : October 12, 1993
INVENTOR(S) : Jong-Seo Hong

It is certified that error appears in the above-indentified patent and that said Letters Patent is hereby corrected as shown below:

Column 2, Line 9, Change "interior" to --inferior-- .

Signed and Sealed this

Nineteenth Day of September, 1995

Attest:

BRUCE LEHMAN

Attesting Officer

Commissioner of Patents and Trademarks